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POSTER

Outlier Screening for IC Based on Sparse Multi-Output Gaussian Process Regression

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ABSTRACT

Outlier screening is essential for semiconductor device reliability. Conventional methods often fail to integrate global and local wafer information and analyze test items in isolation. To address this, we propose a wafer-level anomaly detection framework based on sparse multi-output Gaussian Process Regression (GPR). This method jointly models spatial trends across multiple test items, captures correlations via a low-rank mixing matrix, and ensures computational efficiency through sparsity.

INTRODUCTION

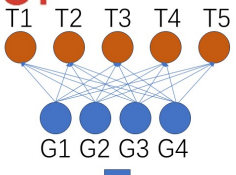
The randomness of a test item can be modeled as the result of multiple environmental factors acting together, such as temperature gradients and gravity gradients. We model different environmental factors as a set of latent Gaussian processes.

Unlike the previous approaches that modeled test items as independent Gaussian processes , this method implicitly reveals the relationships between different test items.

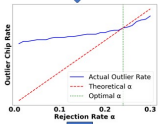
Once the model is sufficiently trained, the mean and variance can be obtained, Next, the residuals can be normalized, Based on the normalized residuals, Anomaly Score for each chip can be derived

METHODOLOGY

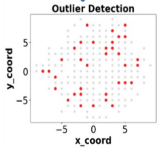
GPR Model for Data Fitting



Finding the Optimal Rejection Rate

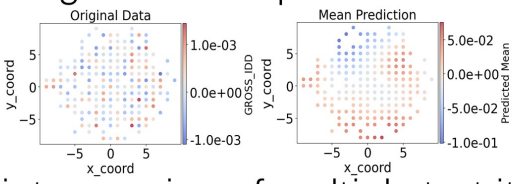


Outlier Screening

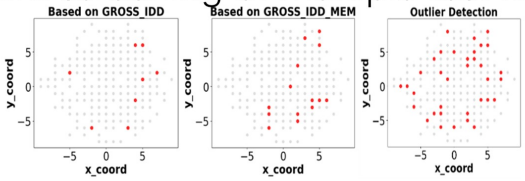


RESULTS & DISCUSSION

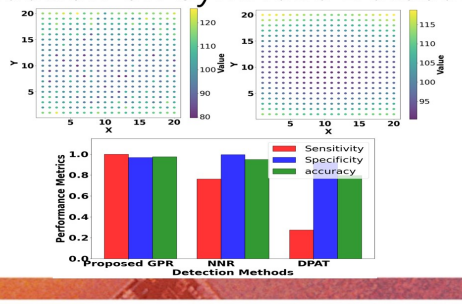
global trend prediction



Joint screening of multiple test items



Validation on Synthetic Datasets



SUMMARY

This paper proposed a wafer-level outlier screening framework based on sparse multi-output Gaussian Process Regression (GPR). Unlike conventional methods that analyze test items in isolation, our approach leverages cross-metric correlations to effectively fuse global wafer trends with local spatial information. Validation on industrial and synthetic datasets confirms that this method outperforms traditional techniques (such as DPAT and NNR) in detecting latent defects. Ultimately, this comprehensive screening framework offers a novel approach for achieving the zero-defect and zero-PPM reliability target in semiconductor manufacturing for reliability critical chips.