Lam RESEARCH

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Gate Etch Pull Back Profile Improved by SiCl4/O2 Cycle Pre-Dep

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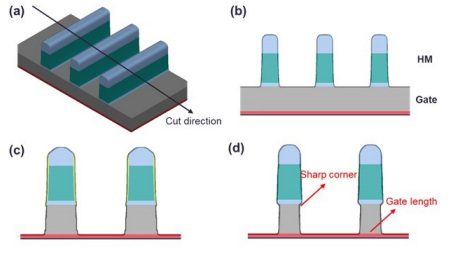
ABSTRACT

Feature sidewall profile pull back (large HM and gate CD delta) is a common issue at gate etch, which is caused by insufficient sidewall protection during gate etch. Traditional methods have tradeoffs with tapered profile or more HM loss. To avoid these tradeoffs, another method to increase incoming mask CD by adding $SiCl_4/O_2$ pre-deposition has been proposed. In this poster, we have found that adding $SiCl_4/O_2$ pre-dep not merely shows benefit for gate pull back profile but also can improve LWR (line width roughness) performance.

INTRODUCTION

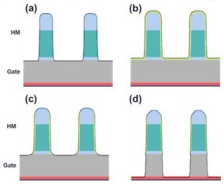
Gate etch 3-Dimensional and 2-Dimensional schematic diagrams are shown in below image (a)(b), and (c) is desired profile with smooth profile transition between HM and gate, with enough HM remaining and vertical gate profile. (d) is typical pull back profile, where gate CD is smaller than HM incoming CD. Gate pull back profile will impact gate CD and hence cause smaller gate length. $SiCl_4/O_2$ coating is a commonly used method at WAC (waferless auto clean) process, with the reaction equation of $SiCl_4 + O_2 \rightarrow SiO_2 + 2Cl_2$. We have applied $SiCl_4/O_2$ coating at gate etch to improve pull back profile, where the deposited thin SiO_2 layer can enlarge HM CD and hence improve gate pull back profile.



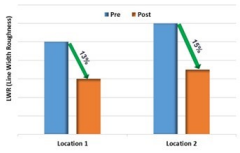
RESULTS & DISCUSSION

The illustration of $SiCl_4/O_2$ pre-deposition process is shown in below right image. $SiCl_4$ reacts with O_2 to form SiO_2 and deposits on HM, which is useful to enlarge HM CD. Due to the directionality of dry etch, the vertical etching rate is much faster than the lateral etching rate. As of such, increased HM CD can mitigate the gate sidewall pull back while still with adequate HM remaining.

Adding $SiCl_4/O_2$ pre-deposition is useful to mitigate pull back, while not impacting gate profile and the final HM remaining.



Adding $SiCl_4/O_2$ pre-deposition also shows benefit for LWR. This is because $SiCl_4/O_2$ cyclic deposition can reduce incoming HM sidewall roughness. As shown in left image, based on top view of CD-SEM data, with $SiCl_4$&O_2 pre-deposition the LWR can be improved at different locations.



SUMMARY

In this study, a $SiCl_4/O_2$ pre-deposition method is proposed to improved gate sidewall pull back during etch process. $SiCl_4/O_2$ pre-deposition method is useful to break through the tradeoffs with tapered profile or more HM loss. Additionally, adding $SiCl_4/O_2$ pre-deposition shows benefit on LWR reduction. Better LWR means more smooth gate profile, which is beneficial for final electrical properties and reduced leakage. This poster shared an experience about gate pull back profile improvement.

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