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A 240 × 160 18-bit SPAD HDR Imaging Chip Using 3D-Stacked Technology

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ABSTRACT

This work presents a 240×160 SPAD HDR imaging chip fabricated with 3D-stacked integration and achieves a 100.24 dB single-frame dynamic range.

Key Innovations:

1. Per-pixel independent gated quenching circuit & 18-bit counter to suppress noise.
2. 100 MHz gated clock strategy for high-speed quenching, reducing dead time and after-pulsing.

INTRODUCTION

Background: SPADs offer exceptional precision for single-photon detection but face challenges in dynamic range and noise in complex environments.

Challenge: Conventional architectures struggle with clock saturation and limited counting depth in high-flux scenarios.

Our Contributions:

- 3D-Stacked Architecture: Integrates a 240×160 pixel array with per-pixel 18-bit counters.
- Novel Gating Strategy: Implements a 100 MHz high-frequency gating to mitigate clock saturation.
- HDR: Demonstrates a record 100.24 dB single-frame dynamic range.

METHODOLOGY

3D Integration:

- The chip employs 3D-stacked technology, vertically interconnecting the SPAD pixel wafer and the front-end circuit wafer through Cu-Cu bonding.

Pixel Circuit Design:

A. Gated Quenching: The quenching circuit is controlled by the EN (enable) and clk_gate (gated clock) signals. It operates with high impedance during the photon detection phase to facilitate quenching, and switches to low impedance for rapid circuit reset.

B. 18-bit Counter: An 18-bit counter is integrated within each pixel. This in-pixel design minimizes noise introduced by downstream data processing and readout circuits.

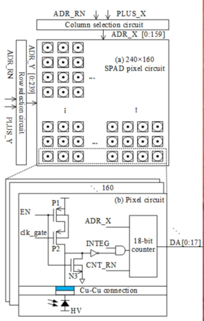


Fig.1. Chip Architecture.
(a) 240×160 pixel circuits for each SPAD pixel.
(b) Pixel circuit.

RESULTS & DISCUSSION

The control system (Fig. 2) employs an Altera Cyclone IV FPGA as the core processing unit, generating all timing signals and managing data acquisition.

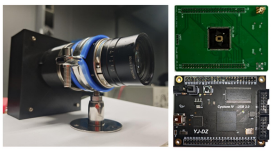


Fig.2. SPAD HDR Imaging System.

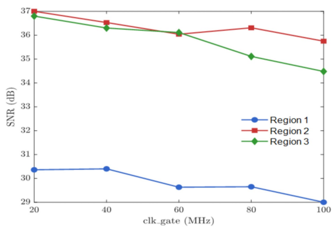
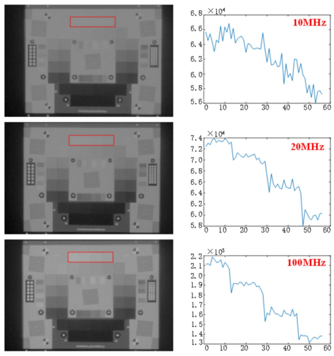


Fig.3. Trend of SNR

Effect of clk_gate Frequency on Imaging Performance.

1. As illustrated in Fig. 3, the influence of the clk_gate frequency on the overall image quality is limited within a given exposure time.



2. As shown in Fig.6, clock saturation is observed in the two brightest patches at 10 MHz. At 20 MHz, no saturation occurs across any patch. At 100 MHz (corresponding to a clock period of 10 ns) all patch counts remain well below the saturation threshold.

Fig.4. Imaging performance under varying clk_gate frequencies.

SUMMARY

The dynamic range (DR) is quantified using:

$$DR(db) = 20\log_{10}(\frac{Max}{Min})$$

where Max denotes the mean photon count of the brightest patch in the test chart, and Min corresponds to that of the darkest patch.

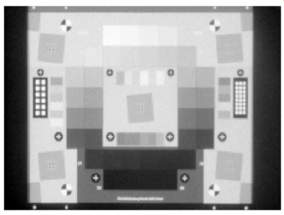


Fig.5. Display of the Original Image Following Logarithmic Transformation.

As shown in Fig. 5, under a clk_gate frequency of 100 MHz and an exposure time of 4 ms, a single-frame image with a dynamic range of 100.24 dB is achieved when the 18-bit photon counter approaches saturation.

This study demonstrates that high dynamic range can be achieved in single-photon imaging systems through optimized clock-gating strategies and photon counting, offering a viable technical pathway for demanding applications