A Novel Silicon Fin-TFET Technology Based on Foundry Platform

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ABSTRACT

In this work, Si Fin-TFET that can monolithically integrate on baseline platform is designed for the first time. This Si Fin-TFET is designed with an asymmetrical structure to enable a self-aligned, SiGe-based, highly doped source overlap region for high performance and a drain underlap region for low power consumption. Compared with planar TFET which can also monolithically fabricated on baseline platform, the optimized Fin-TFET achieves higher I_{ON} and lower V_{DD} without sacrificing I_{OFF}, demonstrating its potential for device scaling.

MOTIVATION

While BTBT-based Si TFETs offer excellent OFF-state characteristics, performance optimization of Fin-TFETs under CMOS-compatible foundry processes remains underexplored.

Device Structure and Simulation Schemes

- Proposed Fin-TFET features an asymmetrical spacer and highly doped SiGe S/D.
- TCAD parameters are strictly calibrated with experimental data.

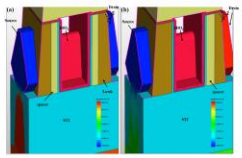

Figure 1: Simulation structures of (a) FinFET and (b) Fin-TFET in Sentaurus TCAD.

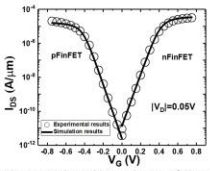

Figure 2: The calibrated I_D-V_G of FinFETs are matched well with experimental result

Design Process flow for Fin-TFET Integration on Baseline Platform

☐ **Process flow to integrate Fin-TFET on baseline platform**

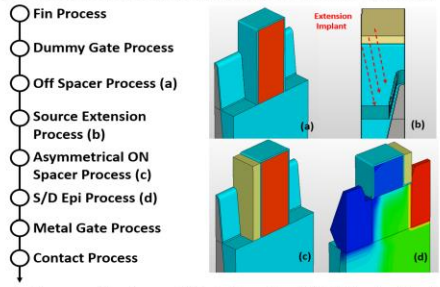

Figure 3：The process flow for monolithically integration of Fin-TFET on baseline platform.

- Highly-doped SiGe S/D for performance enhancement while sharing process between n-TFET source and p-TFET drain for cost-saving.
- **Self-aligned asymmetrical spacer** through source-side ON spacer etch for high I_{ON}/I_{OFF} with ultra-low I_{OFF}.

☐ **Results after optimization**

- **The optimized Fin-TFET exhibits higher I_{ON} and lower V_{DD} compared to baseline planar TFETs without leakage penalty**, showing the potential of Fin-TFET for device scaling.

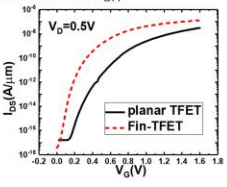

Figure 4：The I_D-V_G curves of planar and Fin-TFET.

Design Optimization of Si Fin-TFET

☐ **Reducing λ and E_G is critical performance enhancement**

$$I_{DS} \propto \exp\left(-\frac{4\lambda\sqrt{2m^*}E_G^{2/3}}{3q\hbar\left(E_G+\Delta\Phi\right)}\right) \qquad SS \propto \ln 10\left[\frac{4\sqrt{2m^*}E_G^{1/2}}{3q\hbar}\left|\frac{\partial\lambda}{\partial V_{GS}}\right|\right]^{-1}$$

☐ **Strategy I: Source overlap design for smaller λ**

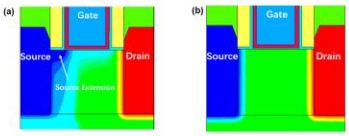

Figure 5: Device structure of Fin-TFET (a)with and (b)without gate-source overlap region.

- **Device Physics:** Highly doped gate-source overlap region can result in a smaller λ to enhance I_{ON} and sharpen SS.
- **Process Design:** an additional mask is used to shield the drain region, enabling **high-dose implantation exclusively at the source-side** source/drain extension (SDE) region before ON spacer formation to create the highly-doped gate-source overlap structure.
- **Simulation Results:** The **I_{ON}** of the **n-type Fin-TFET** is enhanced **by 54.8×,** and the **I_{ON}** of the **p-type Fin-TFET** is enhanced by **12.9×**. Furthermore, the SS values for both devices are also reduced.

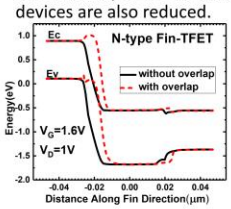

Figure 6: The energy band diagrams for nFin-TFET w/ and w/o the gate-source overlap.

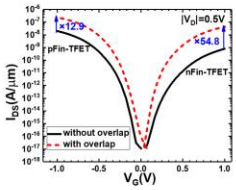

Figure 7：The I_D-V_G curves of n-type and p-type Fin-TFETs w/ and w/o the gate-source overlap..

☐ **Strategy II: Source material design for smaller E_G**

- **SiGe** is utilized for its **narrow E_G and CMOS compatibility**.
- Compared with Si Fin-TFETs, Fin-TFET with SiGe source enhances the I_{ON} of n- and p-type Fin-TFETs by **75.1 & 73.3** times, respectively.

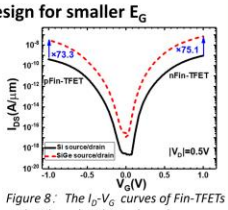

Figure 8：The I_D-V_G curves of Fin-TFETs with Si-based and SiGe-based source.

CONCLUSION

- An asymmetrical Si Fin-TFET is designed with an asymmetrical structure to enable a self-aligned, SiGe-based, highly doped source overlap region for high performance and a drain underlap region for low power consumption.
- Fin-TFET outperforms planar TFET with higher I_{ON}, lower V_{ON}, and steeper SS, providing promising solution for device scaling on logic foundry platform.