FAILURE ANALYSIS AND LOCALIZATION OF CDM INDUCED MICRO DAMAGE IN HIGH SPEED I/O OF ADVANCED FINFET NODES

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ABSTRACT

This study reports CDM (Charged Device Model)-induced micro-damage in advanced FinFET high-speed I/O circuits. Devices subjected to 250V CDM stress exhibited microampere-level leakage current while still passing functional tests, making such damage difficult to detect. Systematic failure analysis localized the defect to gate oxide breakdown in the driver transistor Mn1. Notably, this failure mechanism does not conform to any of the four previously reported CDM failure modes, suggesting a new CDM-induced damage signature. Furthermore, increasing the device area was found to significantly enhance CDM robustness without compromising logic functionality, offering a practical, device-level design strategy for improving reliability in advanced technology nodes.

INTRODUCTION

As semiconductor technology advances into FinFET nodes, electrostatic discharge (ESD) robustness has become a critical factor for high-speed I/O feasibility [1]. Traditional standards established during the planar CMOS era are now overly stringent, particularly under Charged Device Model (CDM) stress. To meet performance targets, high-speed I/O designs impose strict parasitic capacitance constraints, leading many design houses to eliminate secondary protection networks traditionally used for CDM pulse. Consequently, CDM robustness has shifted from a routine check to a primary design constraint.

ESD qualification is based on two checks: (i) I–V characteristic shifts before and after stress and (ii) Automated Test Equipment (ATE) functional results. In advanced nodes, CDM stress often causes minor parameter changes, such as increased leakage, without functional failure. Any I–V shift beyond the specified threshold is considered indicative of latent damage, even if ATE tests pass [2,3].

To identify and localize such "electrical parameter drift while functionality remains intact" cases, a systematic physical failure analysis is required to determine the damage source. For ESD-related failures, the conventional analysis flow typically includes: initial electrical characterization to identify leakage paths; subsequent hot-spot analysis based on the leakage path to narrow down the suspected circuit region; progressive delayering to the device layer (where CDM stress commonly causes gate damage); electrical localization at the device layer; and finally, cross-sectional verification to confirm the findings. Accurately identifying the defective device under FinFET technology remains a significant challenge, particularly when CDM damage manifests only as microampere-level leakage.

This study focuses on localizing CDM-induced micro-damage in an advanced FinFET technology chip. Using a systematic failure-analysis approach combined with multiple electrical verification techniques at the device layer, the defective MOS transistor was identified, and gate-oxide breakdown was observed. The failure site was located within the I/O driver circuit. By correlating circuit analysis with experimental evidence, the CDM discharge path was clarified, and mechanism inference indicated that the failure mode does not match any of the four commonly recognized CDM failure modes [4]. Further experiments demonstrated that increasing device area significantly improves CDM robustness without altering circuit logic. This work proposes a design optimization strategy that enhances CDM reliability while preserving logic functionality, providing valuable guidance for ESD protection in next-generation high-speed I/O chips

FAILURE ANALYSIS

A. IV Characterization

Three chips were subjected to CDM stress at 250 V. Two devices exhibited significant I–V shift in their high-speed I/Os, exceeding the industry limit of ±30% within the 5 µA leakage boundary. As shown in Fig. 1, the white envelope represents the ±30% tolerance derived from the pre-stress I–V curve, while the post-stress IV curve clearly surpasses this boundary.

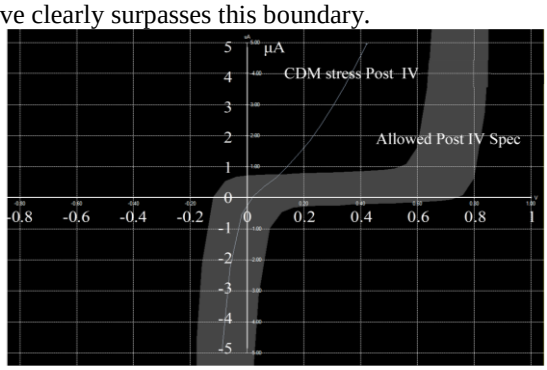

Figure 1: I–V Curve Manifestation for Chips Failed at CDM 250 V

For I/O pins, IV testing before and after CDM stress cannot reveal the exact leakage path. Therefore, electrical

characterization must traverse all possible paths. Verification showed a tenfold increase in leakage toward AVDD08_TX, along with a smaller rise toward AVDD12. Based on the I/O protection schematic (Fig. 2), where the ESD protection diode is directly connected to AVDD08_TX, this domain was identified as the dominant leakage path, guiding subsequent hot-spot localization.

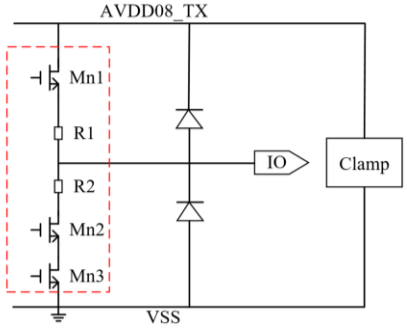

Figure 2: Simplified high-speed I/O schematic

B. Hot-Spot Localization Using OBIRCH

Optical Beam Induced Resistance Change (OBIRCH) was selected as the hot-spot localization technique. Bias was applied along the path from the I/O to AVDD08_TX during scanning. Both the reference and failed chips exhibited a hot-spot at the ESD diode, which is reasonable under a bias voltage of 0.8 V. However, the failed chip showed an additional hot spot in the I/O driver circuit (Fig. 3b), which was absent in the reference device (Fig. 3a). Layout correlation confirmed that this abnormal hot spot corresponds to the I/O driver circuit, specifically the region outlined by the red dashed box in Fig. 2.

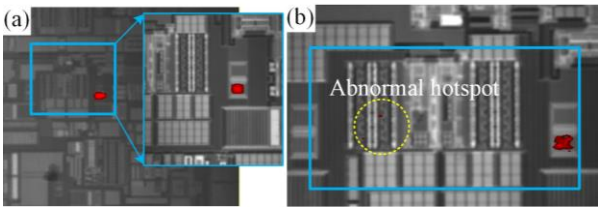

Figure 3: (a) Hot-spot in the reference chip; (b) hot-spot in the failed chip. The failed chip exhibits an additional hot-spot in the I/O driver circuit.

C. Precise Localization on Driver Circuit Using PVC

Failure localization narrowed the suspect region to the I/O driver circuit rather than the ESD protection diode. After delayering to the MD layer, the components in the I/O driver circuit became electrically isolated, preventing further refinement through global testing. Passive Voltage Contrast (PVC) was then used for precise localization. At 0.5 kV landing energy (Fig. 4), several Mn1 transistors exhibited distinct contrast; for example, the right vias at position 1 appeared bright, the left vias appeared dark, and all vias at position 2 were uniformly dark. Based on PVC principles, floating structures accumulate charge and appear dark, while grounded structures remain bright. These results suggest a leakage path from the gate to the substrate beneath the bright via at position 1.

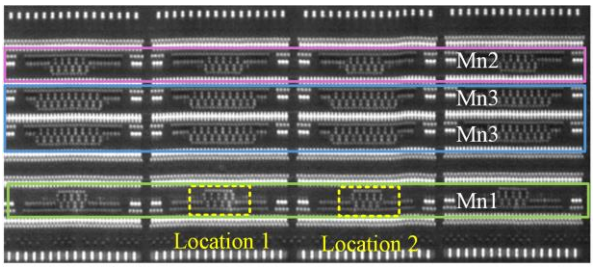

Figure 4. PVC revealing Mn1 anomaly

D. Defect Confirmation Using Nanoprobe

To confirm the defect, nanoprobe characterization was performed on devices at positions 1 and 2. Bias-scan results showed a significant reduction in gate-to-source/drain impedance on the right side of position 1 compared with its left side and position 2, indicating a localized conductive path in the gate oxide. To avoid secondary damage from DC stress, probe current was limited to ±10 µA throughout the analysis.

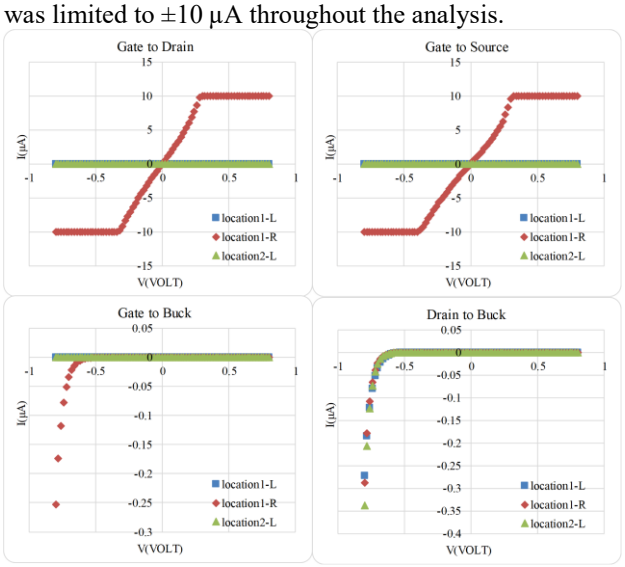

Figure 5: Nanoprobe test results for positions 1 and 2. The left side of position 1 and position 2 exhibit normal impedance characteristics, leading to partial overlap of the data curves.

E. EBIC Verification

EBIC analysis on the right side of position 1 under gate-to-bulk bias revealed contrast anomalies (Fig. 6), confirming the presence of a localized leakage defect.

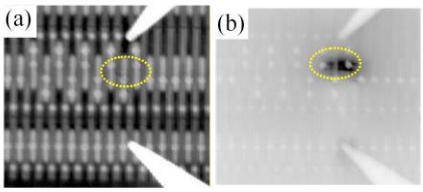

Figure 6: (a) SEM image of position 1;(b) EBIC abnormal image of position1

F. TEM and EDS Analysis

A planar TEM section prepared for position 1 revealed gate breakdown on its right side (Fig. 7). EDS

analysis confirmed tungsten extrusion, fracture of the Ti-based barrier layer, and damage to the HfO_2 high-k dielectric. These findings align with the gate-oxide breakdown–melting model under CDM transient energy, identifying the failure mechanism as local melting damage induced by gate discharge.

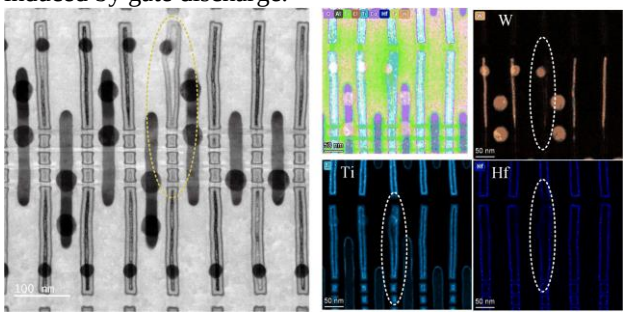

Figure 7: Planar TEM and EDS of position 1

FAILURE LOCALIZATION

Based on the observed failure phenomena, the root cause could not be conclusively determined without verifying the polarity of the CDM stress. To clarify this, three fresh samples were subjected to ±250 V CDM stress. Two samples passed after positive stress but exhibited an I–V shift exceeding 30% following negative stress, while one sample passed under both conditions. These results confirm that failures are polarity-dependent.

Circuit analysis indicates that under a negative CDM pulse, the I/O node is driven to a high potential, and the discharge should ideally occur through the ESD protection diode. However, localization reveals that Mn1 fails first. Schematic analysis shows that a portion of the discharge current flows through Mn1, as illustrated in Fig. 8. Since Mn1's rated pulse current is significantly lower than the CDM peak current, this unintended path rapidly enters avalanche breakdown under high-density transient energy, resulting in localized thermal-electrical damage.

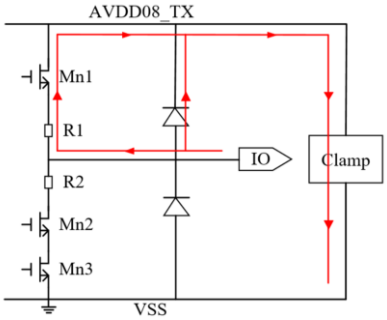

Figure 8: CDM stress current discharge path

To validate the failure mechanism, another fresh sample was stressed at ±500 V CDM. PVC analysis of this sample (Fig. 9) revealed that, in addition to Mn1, Mn2 also failed under this condition, indicating that the number of failed devices increases with stress voltage. Although Mn1 and Mn2 share identical device structures, their layout sizes differ. This observation suggests that Mn2, with its larger area, can sustain a higher failure current and thus exhibits greater robustness.

Increasing the device area is a feasible approach to improve CDM tolerance without significantly impacting circuit performance. Simulation results confirm that enlarging Mn1 does not degrade circuit performance. Therefore, this method offers both technical feasibility and practical engineering value.

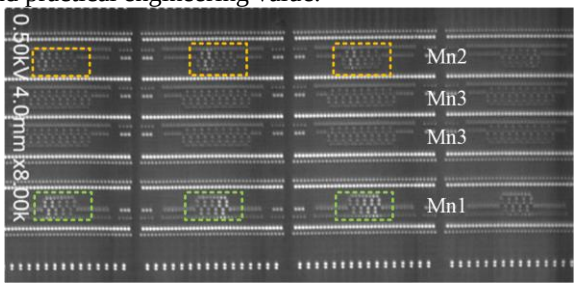

Fig. 9.PVC image of the CDM-500 V failed chip, showing abnormalities in both the Mn2 and Mn1 regions.

CONCLUSION

Through systematic failure analysis, this study identifies gate-oxide micro-breakdown in Mn1 as the root cause of microampere-level leakage under CDM stress in advanced FinFET nodes. Mechanism analysis reveals that an unintended discharge path through Mn1 leads to localized thermal-electrical damage. Experimental results confirm a positive correlation between device area and CDM robustness, demonstrating that larger layouts sustain higher transient currents. These findings clarify the underlying mechanism of CDM-induced micro-damage and provide a practical optimization approach for ESD design in next-generation high-speed I/O circuits.

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