ADVANCED 2NM NODE NANOSHEET FET COMPACT MODEL BASED ON ARTIFICIAL NEURAL NETWORK

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ABSTRACT

In this paper, we have developed a novel, simplified SPICE model for Nanosheet FET that requires no physical formula to drive it, necessitating only the input of corresponding data. Results demonstrate that our ANN model, which employs specialized pre-processing and post-processing, accurately fits both DC and AC curves from TCAD simulation of 2nm node Nanosheet FET. This model can replace the traditional BSIM-CMG model while achieving high precision. The fitting error of off-state and on-state current is reduced by 40.3% and 7.8% respectively against TCAD results, compared to the BSIM-CMG model. The developed model is further implemented in Verilog-A and used for inverter and ring oscillator (RO) simulations in SPICE. Moreover, in an 11-stage RO simulation with V_{dd} at 0.65V, static leakage current is 40.79% higher from simulation with BSIM-CMG model compared to that with ANN model, while frequency is 7.55% lower. This aligns closely with fitting error results in device models.

INTRODUCTION

Over the past half-century, driven by Moore's Law, integrated circuits have advanced rapidly. CMOS device process nodes have continuously scaled, gradually introducing new technologies and structures such as high-k/metal-gate, SMT stress, FDSOI, FinFET, Nanosheet FET, CFET, etc. These innovations have increased the complexity of SPICE models and necessitate consideration of numerous parasitic effects and short-channel effects. As SPICE models serve as the critical bridge between process technology and design, they are essential to the precise simulation of integrated circuits and design-technology co-optimization (DTCO) [1]. The most widely recognized model in the industry is the BSIM model which is guided by physical equations [2]. The most advanced BSIM models, including BSIM-IMG and BSIM-CMG, are widely adopted for FD-SOI, FinFET and nanosheet FET [3]. These complex SPICE models are used for designers to create superior PPAC (Performance Power Area Cost).

However, traditional BSIM models based on device physics equations require extensive specialized knowledge. Consequently, modeling these emerging devices using traditional methods becomes extremely difficult and time-consuming [4]. Therefore, owing to the powerful training capabilities of artificial neural networks, models based solely on device electrical data without incorporating physical knowledge have gradually attracted attention due to high precision and simplicity of application [5][6]. In this paper, we have developed a nanosheet FET SPICE model based on artificial neural network that requires only data input without physical formula. Through specialized pre-processing and post-processing of current and capacitance data, this model accurately fits the relationships of current-voltage (I-V) and capacitance-voltage (C-V). The developed model is further implemented in Cadence via Verilog-A for inverter and ring oscillator.

MODEL DEVELOPEMENT

Figure 1 illustrates the complete model development workflow of the BSIM-CMG and ANN model. TCAD simulation is first conducted to obtain DC and AC data used for model training. The simulated nanosheet FET calibrated against the HP (high performance) data from IRDS [7], with L_g at 14nm, W_{ns} at 30nm, triple-layer nanosheets, nanosheet thickness of 6 nm. The composition of the ANN model is shown in Figure 1, which comprises six inputs and three outputs. ANN training requires preprocessing and postprocessing, which is implemented in python. Upon completion of ANN model training, it is implemented in Verilog-A for SPICE simulation.

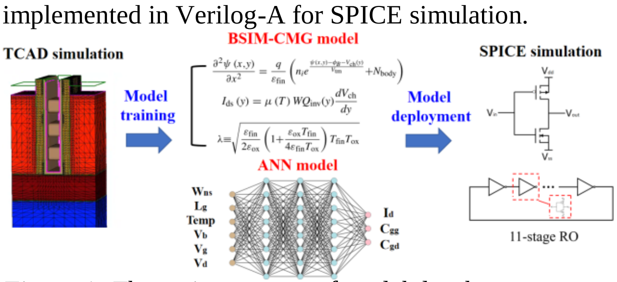

Figure 1: The entire process of model development

Figure 2 presents the AC fitting results for n-type and p-type nanosheet FETs using BSIM-CMG and ANN models. Figure 2(a) and (c) present the C_{gg}-V_g results of the n-type and p-type. Figure 2 (b) and (d) show the zoom-in results on specific regions, in which ANN model demonstrates greater precision than BSIM-CMG model. The fitting error of n-type and p-type reduces approximately 2% compared to BSIM-CMG model.

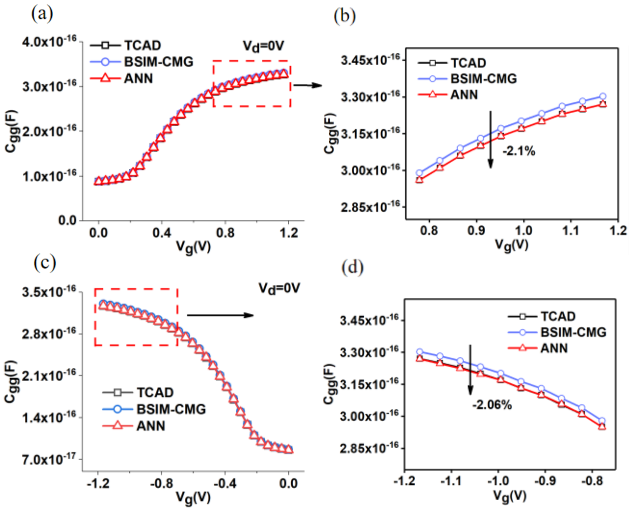

Figure 2: (a) BSIM-CMG and ANN model comparison of C_{gg}-V_g characteristics on a nFET. (b) Enlarged area in (a). (c) BSIM-CMG and ANN model comparison of C_{gg}-V_g characteristics on a pFET. (d) Enlarged area in (c).

Figure 3 presents the DC fitting results of n-type nanosheet FET using BSIM-CMG and ANN models. Figure 3(a) displays the comparison of n-type I_d-V_g curve. Figure 3(b) depicts the zoom-in result near the off-state. The fitting of ANN model is accurate in both ON and OFF states, whereas the current of BSIM-CMG model exhibits significant error up to 40% in OFF state.

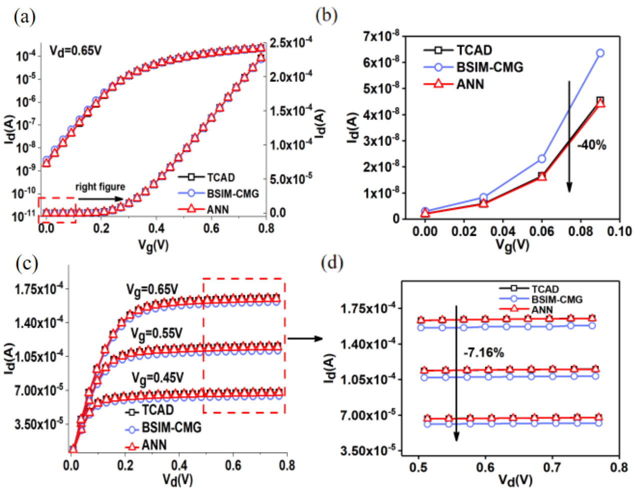

Figure 3: (a) BSIM-CMG and ANN model comparison of I_d-V_g characteristics on a nFET. (b) Enlarged area in (a). (c) BSIM-CMG and ANN model comparison of I_d-V_d characteristics on a nFET. (d) Enlarged area in (c).

Figure 3(c) displays the comparison of I_d-V_d curves from nFET. Figure 3(d) depicts the zoom-in results on saturation region. The fitting error of BSIM-CMG model in ON state is not particularly large, approximately 7%. Figure 4 displays the results of the pFET DC fitting. Similar to the n-type results, a significant fitting error is observed in OFF state, and a minor fitting error is observed in ON state.

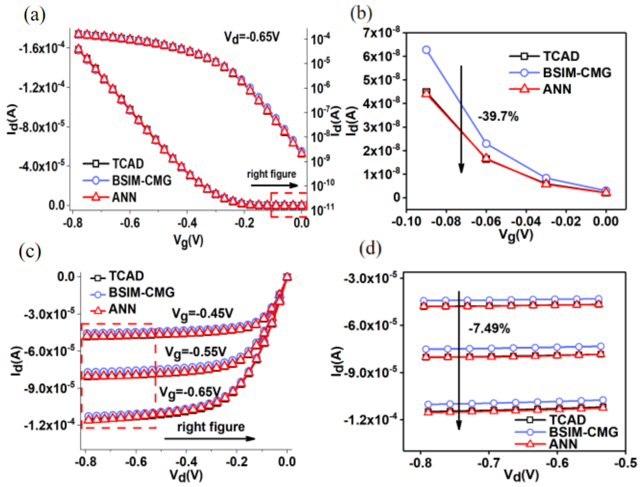

Figure 4: (a) BSIM-CMG and ANN model comparison of I_d-V_g characteristics on a pFET. (b) Enlarged area in (a). (c) BSIM-CMG and ANN model comparison of I_d-V_d characteristics on a pFET. (d) Enlarged area in (c).

Subsequently, we present the fitting error of the BSIM-CMG and ANN model against TCAD data across the entire range of I_d from 10^{-9} to 10^{-5} (A) and C_{gg} from 10^{-17} to 10^{-14} (F), including both n-type and p-type data. As anticipated, Figure 5(a) reveals that the ANN model exhibits minimal errors in both on-state and off-state currents. In contrast, the BSIM-CMG model shows errors of 40.3% and 7.8% OFF and ON states compared to ANN model. In Figure 5(b), both BSIM-CMG and ANN model exhibit low overall errors of capacitances, in which BSIM-CMG model has 2.14% higher than ANN model.

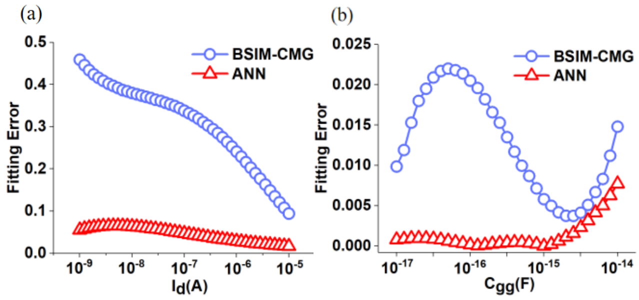

Figure 5: (a) Comparison of I_d fitting error between BSIM-CMG and ANN model within the range from 10^{-9} to 10^{-5} (A). (b) Comparison of C_{gg} fitting error between BSIM-CMG and ANN model within the range from 10^{-17} to 10^{-14} (F)

CIRCUIT SIMULATION

The developed models are subsequently implemented in Verilog-A and used in SPICE for circuit simulation. The following inverter and ring oscillator simulations demonstrate the application of the ANN model. Figure 6(a) displays the transient simulation of an inverter with a supply voltage V_{dd} of 0.65V. Subsequently, an 11-stage ring oscillator is simulated using the inverter from Figure 6(a) for transient simulation. The result is shown in Figure 6(b). Due to variations in on-state current causing frequency shifts, the frequency of the simulation based on the ANN model is 114.62 GHz, while that based on the BSIM-CMG model is 106.57 GHz, which is 7.55% lower than that based on ANN model.

To further demonstrate the advantages of ANN model in off-state current, a SPICE simulation is conducted on the static leakage of an 11-stage ring oscillator composed of NAND and Inverter. The final results indicate that at V_{dd} of 0.65V, the static leakage of the simulation based on ANN model is 1.998nA, while that based on the BSIM-CMG model is 2.813nA, which is 40.79% higher than the results simulated with ANN model.

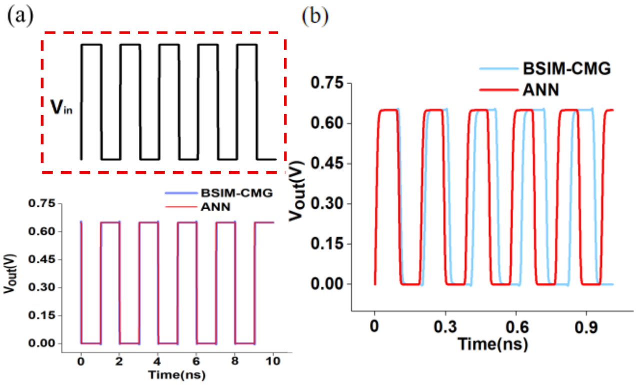

Figure 6: (a) Waveform comparison of inverter transient simulation using BSIM-CMG and ANN model (b) Waveform comparison of 11-stage ring oscillator transient simulation using BSIM-CMG and ANN model.

CONCLUSION

We have successfully developed a simplified Nanosheet FET SPICE model. Through unique pre-processing and post-processing methods, the DC and AC characteristics of n-type and p-type nanosheet FETs are modeled with ANN model. Based on calibrated TCAD simulation, we conduct I_d and C_{gg} fitting error analyses against BSIM-CMG model. Results indicate that while BSIM-CMG and ANN model exhibit comparable fitting error of C_{gg}, however, compared to BSIM-CMG model, the ANN model reduced the fitting errors for off-state and on-state currents by 40.3% and 7.8% respectively. Subsequently, the ANN model is converted into Verilog-A language and embedded within Cadence for inverter and ring oscillator simulation. To further demonstrate the advantages of ANN model in both on-state and off-state current performance, we compare the frequency and static leakage of the ANN model and BSIM-CMG model in 11-stage RO simulation. Results indicate that the frequency of the simulation based on BSIM-CMG model is 7.55% lower than that based on ANN model, while the static leakage current of the simulation with BSIM-CMG model is 40.79% than the results simulated with ANN model This aligns closely with observed fitting error in device level. Owing to its simplicity and high precision, ANN holds promising prospects for broader application in device modelling at more advanced process nodes.

ACKNOWLEDGEMENTS

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