A NOVEL ANTI-FERROELECTRIC FET BASED SCHMITT TRIGGER WITH LOW OPERATING VOLTAGE AND HIGH HARDWARE-EFFICIENCY

Bingrui Song[1], *Jin Luo*[1*], *Runze Han*[1], *Qianqian Huang*[1,2*] *and Ru Huang*[1,2*]
[1]School of Integrated Circuits, Peking University, Beijing 100871, China
[2]Beijing Advanced Innovation Center for Integrated Circuits, Beijing 100871, China
*Corresponding Author's Email: luoj@pku.edu.cn, hqq@pku.edu.cn, ruhuang@pku.edu.cn

ABSTRACT

In this work, a novel anti-ferroelectric (AFE) FET (AFeFET) based Schmitt trigger (ST) is proposed for the first time, targeting low-voltage and hardware-efficient signal conditioning. By utilizing the intrinsic hysteresis from volatile polarization switching in AFE materials, the AFeFET-based ST (AFEST) realizes hysteresis of dual positive thresholds with only two transistors. Circuit simulations based on AFeFET modeling illustrate principles of the designed AFEST. Furthermore, using a fabricated AFeFET with ZrO_2 gate layer, the AFEST is experimentally demonstrated to perform multiple signal processing functions, including waveform transforming, noisy signal filtering, and pulse amplitude discrimination. Owing to lower coercive field of AFE materials, the proposed ST achieves a lower operating voltage than conventional ferroelectric hysteresis based STs, showing strong potential for low-power signal conditioning in edge applications.

INTRODUCTION

Schmitt triggers (STs), which utilize hysteretic behavior to achieve noise immunity, are widely used in signal processing for edge applications [1-2]. Conventional CMOS-based ST implementations typically rely on inverter-based 6T or 4T2R circuits to generate hysteresis (Fig. 1a) [3]. Recently, by leveraging ferroelectric polarization hysteresis, ferroelectric FETs (FeFETs) have emerged as a promising alternative for realizing STs with lower hardware overhead [4-6]. Such FeFET-based STs (FESTs) have been demonstrated using ferroelectric (FE) inverters with IGZO [4], organic [5] and carbon nanotube [6] channels. However, due to the non-volatility and bipolar coercive field (E_c) of FE domains, the FESTs generally require bipolar operating voltage with high amplitude (Fig. 1b), resulting in limited practicality and high energy consumption.

In this work, a novel anti-ferroelectric (AFE) FET (AFeFET) based ST (AFEST) is proposed and experimentally demonstrated with only two transistors. By exploiting the intrinsic volatile hysteresis with low E_c in AFE materials, the ST with dual positive thresholds is realized using an AFeFET-based inverter, and shows robust signal processing capabilities under a low operating voltage.

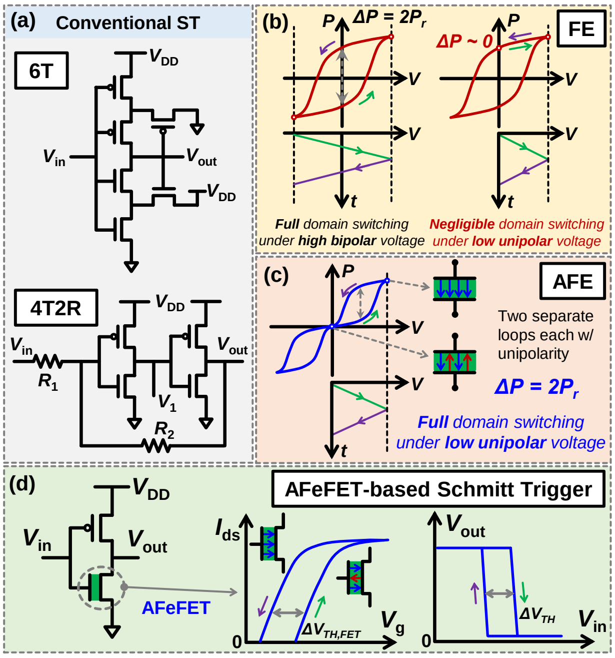

Figure 1: (a) Conventional 6T and 4T2R implementations of Schmitt trigger (ST). Schematic diagram of (c) AFE polarization switching compared with that of (b) FE. (d) The proposed AFeFET-based 2T ST (AFEST) design with hysteresis of dual positive threshold voltages (V_{TH}).

DESIGN OF THE AFEST

Under low unipolar voltage sweeping, AFE materials with low E_c demonstrate full domain switching and provide polarization difference of $2P_r$ while P_r is quasi-remanent polarization of single hysteresis loop (Fig. 1c). Due to this behavior, the AFeFET with AFE gate layer exhibits a distinct hysteresis window in transfer characteristics (Fig. 1d), which is promising to serve as hysteretic effect that ST requires. Inspired by this, the proposed AFEST is further constructed utilizing the AFeFET. Its voltage transfer curve (VTC) will demonstrate a dual-positive-threshold hysteresis under unipolar operating voltage with low amplitude.

To analyze the behavior of AFEST, an AFeFET model is first established using BSIM model for the transistor (Fig. 2b) and a novel multi-domain dynamic Preisach model for the AFE capacitor (AFeCap) (Fig. 2a). AFeCap

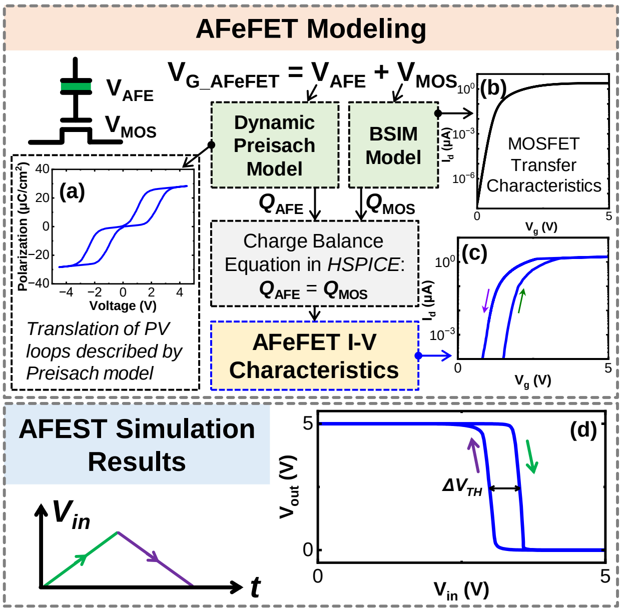

Figure 2: (a) PV loop of AFeCap described by multi-domain dynamic Preisach model. (b) MOS transfer characteristics described by BSIM model. (c) Simulated AFeFET I-V characteristics with hysteresis. (d) Simulated voltage transfer characteristics (VTC) of AFEST with hysteresis window.

exhibits two separate hysteresis loops under positive and negative voltage, respectively, each follows polarization switching principles which could be described by our previous Preisach model [7] after translation. Our insights of the novel AFeCap model are to capture AFE polarization switching behavior by combining the two translated separate loops together. Furthermore, I-V characteristics of AFeFET are calculated based on charge balance equation, revealing a pronounced hysteresis window under unipolar gate voltage (V_g) sweep (Fig. 2c).

Leveraging the AFeFET model, the proposed AFEST is constructed and simulated in HSPICE (Fig. 2d). In rising stage of input voltage (V_{in}), AFeFET exhibits a high threshold voltage as AFE remains at relatively low polarization state, leading to a high V_{TH} of AFEST. In the following falling stage of V_{in}, as AFE polarization switching has been taken place, AFeFET demonstrates a low threshold voltage due to the relatively high AFE polarization state, leading to a low V_{TH} of AFEST. The AFEST enables lower amplitude of V_{in} than previous FESTs, since lower voltage is required to switch AFE polarization.

AFEST BEHAVIOR

Based on the design, AFeFET devices are fabricated for AFEST circuit construction. Versatile signal processing capabilities of AFEST are also experimentally demonstrated for further validation.

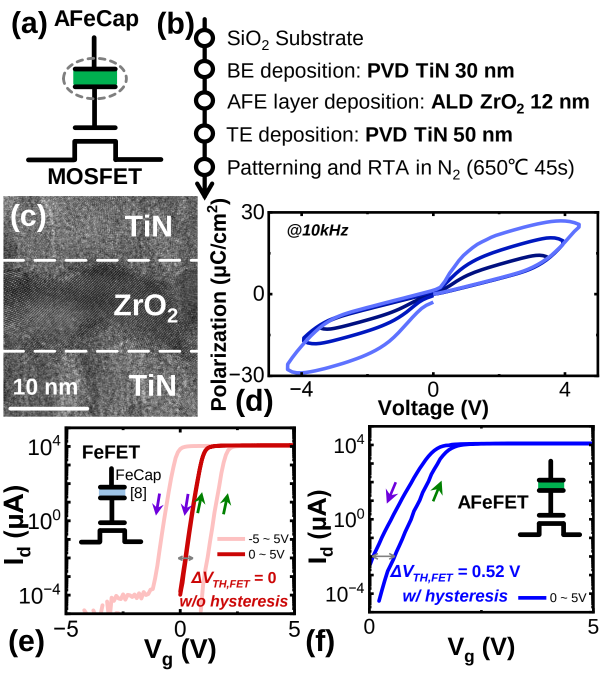

Figure 3: Experiments and characteristics of (a) AFeFET. (b) Process flow and (c) HRTEM image of fabricated ZrO_2 AFeCap. (d) AFeCap PV characteristics under different operating voltages. Transfer characteristics of (e) FeFET showing no hysteresis and (f) AFeFET showing remarkable hysteresis under low unipolar V_g sweep.

AFeFET fabrication and characteristics

AFeCap is firstly fabricated and then connected in series with the gate of an NMOS to construct the AFeFET (Fig. 3a). The AFeCap fabrication process involves sequentially depositing 30 nm TiN by physical vapor deposition (PVD), 12 nm ZrO_2 by atomic layer deposition (ALD), and 50 nm TiN by PVD. After patterning, rapid thermal annealing (RTA) is performed at 650 °C for 45 s (Fig. 3b). The fabricated AFeCap shows clear interface between TiN and ZrO_2 (Fig. 3c), and exhibits two separate P-V hysteresis loops, each with $2P_r$ of approximately 20 μC/cm^2 (Fig. 3d).

By connecting previously fabricated FeCap [8] in series with the gate of an NMOS, a FeFET for comparison is constructed and shows no hysteresis under low unipolar V_g sweep condition (Fig. 3e), indicating invalidity of conventional FESTs for low unipolar signal processing. In contrast, the AFeFET exhibits remarkable hysteresis of 0.52 V under the same V_g sweep (Fig. 3f), making AFEST to be a promising candidate in the same case.

AFEST functionalities for signal conditioning

Based on the fabricated AFeFET, AFEST is constructed with one AFeFET and one PMOS, and its behaviors are measured using Keysight B1500A semiconductor characterization system and oscilloscope (Fig. 4a). For

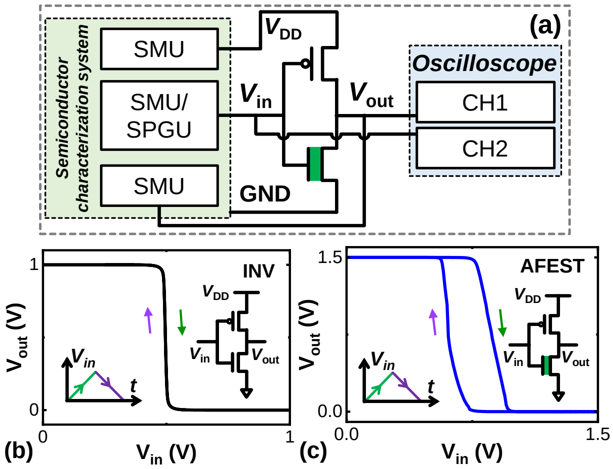

Figure 4: (a) Measurement setup of AFEST. Measured VTC of (b) basic inverter (INV) and (c) AFEST.

comparison, an inverter (INV) composed of one NMOS and one PMOS, as well as a FEST composed of one FeFET and one PMOS, are also constructed. The measured VTC of AFEST shows a hysteresis window resulting from volatile AFE polarization switching (Fig. 4c), while INV shows no hysteretic behavior (Fig. 4b). Furthermore, compared with INV and FEST, versatile functions of AFEST are experimentally demonstrated under a low unipolar operating voltage:

(i) Waveform transforming (Fig. 5a): Converting signals (e.g., triangular wave) into square wave is necessary in some cases. While all of the AFEST, FEST, and INV accomplish, only the AFEST exhibits a stable difference between its rising-edge and falling-edge threshold voltages. This indicates that only AFEST demonstrates a stable noise margin, due to its hysteresis window originated from volatile polarization of AFE.

(ii) Noisy signal filtering (Fig. 5b): For square-wave signal containing overshoot components, the noise must be filtered to obtain a stable output. Due to their negligible noise margin, both the inverter and FEST involve spike pulses or glitches in output waveform. In contrast, the AFEST with inherent noise margin generates a clean square wave, demonstrating effective noise immunity.

(iii) Pulse amplitude discrimination (Fig. 5c): Only pulses with an amplitude higher than the threshold produce a low-level (0 V) output, enabling their discrimination. Lacking a threshold window, the inverter and FEST may produce intermediate output voltage levels between 0 and V_{DD} for pulses with amplitudes close to their unique threshold, leading to failed discrimination. In contrast, the AFEST featuring a distinct threshold window robustly outputs a solid low level to successfully identify pulses exceeding the threshold, demonstrating robust amplitude discrimination capabilities.

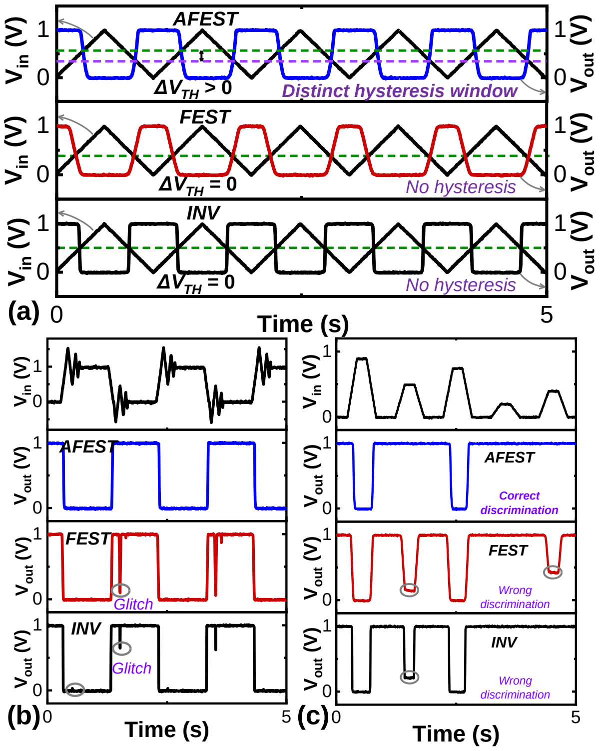

Figure 5: Measured output waveform of AFEST, FEST, and INV in versatile signal processing functions: (a) waveform transforming, (b) noisy signal filtering and (c) pulse amplitude discrimination.

SUMMARY

This work reports a novel low-operating-voltage AFEST with low hardware cost of only two transistors. Leveraging intrinsic volatile hysteresis of AFE materials, the AFEST realizes dual positive thresholds confirmed by circuit simulations based on AFeFET modeling as well as experiments based on AFeFET fabrication. Further demonstrating its robust signal processing capabilities, the proposed AFEST shows great potential for low-power signal conditioning in edge applications with high hardware-efficiency.

ACKNOWLEDGEMENTS

This work was supported by NSFC (62404008, 62374009), 111 Project (B18001).

REFERENCES

[1] Z. Huang, *et al.*, *TCAS-II*, 2022.
[2] J. F. Sulzbach, *et al.*, in *RTSI*, pp. 1-6, 2022.
[3] C.-W. Lin, *et al.*, in *ISQED*, 2015.
[4] R. Zhao, *et al.*, *EDL*, 2022.
[5] S. Hwang, *et al.*, *Adv. Electron. Mater.*, 2020.
[6] M. K. Q. Jooq, *et al.*, *TUFFC*, 2022.
[7] Z. Fu, *et al.*, in *CSTIC*, 2020.
[8] Z. Fu, *et al.*, in *IEDM*, 2023.