# A COMPACT MODEL OF NON-VOLATILE FERROELECTRIC TUNNEL FET WITH AMBIPOLARITY FOR IN-MEMORY-COMPUTING BASED EDGE AI

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# ABSTRACT

The novel ferroelectric tunnel FET (FeTFET) with ambipolarity has attracted much attention for area- and energy-efficient edge AI applications. To facilitate the circuit simulation based on the new device, in this work, a compact FeTFET model is established through calculating the ambipolar current based on surface potential and tunneling paths of both the source and drain junctions under all-range of gate bias, and the ferroelectric model based on dynamic Preisach model is also included in the gate stack with non-volatility. Based on the proposed model, the FeTFET demonstrates XNOR operation in one device, showing its high applicability for further FeTFET-based circuit design and simulation.

## **INTRODUCTION**

Tunnel FET (TFET) with band-to-band tunneling (BTBT) mechanism has attracted much attention as one of the most promising candidates for ultralow-power applications due to its steep subthreshold swing [1]. Moreover, by taking advantage of the ambipolar BTBT behavior of TFET [2] and combining CMOS-compatible hafnium oxide based ferroelectric (FE) gate stack, the linearly inseparable problem of XNOR-like logic can be implemented in one single ferroelectric tunnel FET, enabling content addressable memory (CAM) [3] and encryption-embedded multiply-accumulate operation [4] for non-volatile in-memory-computing (nvCIM) based edge AI with potential high area- and energy-efficiency.

To evaluate the performance of FeTFET-based nvCIM circuit, the compact model of FeTFET with both ambipolar behavior and ferroelectric behavior is necessary. However, most TFET-based models were mainly aimed at the logic applications where the ambipolarity behavior is not preferred [5][6], and thus the tunneling current under negative gate-to-source bias ( $V_{gs}$ ) were not considered for the n-type device model.

In this paper, based on our previously developed analytical current and capacitance model of TFET under positive gate bias ([7-9]), we further establish the compact model of FeTFET for the first time. Based on the analysis of the symmetry of surface potential in tunneling junction of drain and source regions, the physical model of ambipolar BTBT current under all-range gate bias (both positive and negative  $V_G \& V_{gs}$ ) is established. Combining with dynamic Preisach model for non-volatile modulation of FE gate stack [10], the compact model of FeTFET is developed in HSPICE, enabling simulation analysis for novel FeTFET-based nvCIM applications.

# MODEL DERIVATION AND ANALYSIS

The modeling method of FeTFET device is shown in Fig. 1(a), and the FE layer is stacked on the gate of the TFET (n-type is considered in this paper as illustrated). By modeling the surface potential in both source and drain regions under all-range  $V_{gs}$ , the ambipolar BTBT current is obtained with analytical tunneling paths, along with source/drain to gate capacitance of TFET structure. Further connecting the dynamic Preisach model based FE layer to the gate of TFET, the FeTFET model is established.



Figure 1: (a)Device structure, equivalent circuit diagram and the modeling method for FeTFET in this work. (b)Modeling results of channel surface potential far from source and drain regions at different gate and drain bias.

### The surface potential model for all-range gate bias

The surface potential  $\varphi_{ch}(V_{gs}, V_{ds})$  of the FeTFET channel far away from the source and drain under non-destructive readout mode, which is modulated by both gate and drain bias, is first calculated for further modeling lateral surface potential  $\varphi_{sf}(x)$  and energy band structure of tunnel junction. Based on our previous  $\varphi_{ch}(V_{gs}, V_{ds})$  model under only positive  $V_{gs}$  [8], the modulation of  $\varphi_{ch}$  by source under negative gate bias is calculated and the analytical  $\varphi_{ch}(V_{gs}, V_{ds})$  under all-range

 $V_{gs}$  and  $V_{ds}$  is obtained by utilizing a nested iteration of a smooth join function (Eq. 1, all the equations are listed at the end of this paper) to ensure the continuation and derivability. Fig. 1(b) shows the model results of  $\varphi_{ch}(V_{gs}, V_{ds})$ . It can be seen that when the  $V_{gs}$  is relatively large,  $\varphi_{ch}$  is modulated by the source or drain potential, and when the  $V_{gs}$  is relatively small, it is linearly related to the gate bias.

Furthermore,  $\varphi_{ch}$  is used as one of the boundary conditions to solve the Poisson equation of the lateral surface potential at both source and drain tunnel junctions. Utilizing the parabolic approximation and Gaussian box method [8][9], the surface potential of source region under all-range  $V_{gs}$  can be obtained firstly (Eq. 2-3). According to the symmetry of surface potential in tunnel junction of drain and source regions, independent coordinates at these regions are set respectively in Fig. 2(a). An equivalent gate voltage parameter  $V_{gs}^{mid} = (V_{ds} + V_s)/2$  is introduced to simplify the calculation of the potential at the drain junction (Eq. 4-5), with the premise of satisfying the boundary conditions and approximately consisting with the differential equations. Due to the condition of surface potential continuity, the width of depletion region  $(L_{d1}, L_{d2})$ can be solved as Eq. 6. Therefore, the surface potential model under all-range  $V_{gs}$  for ambipolar BTBT in FeTFET is established and the modeling results are shown in Fig. 2(b)(c), which indicates dual-modulation effects of  $\varphi_{sf}(x)$ with different gate and drain bias [7].



Figure 2: (a) Schematic diagram of the lateral surface potential  $\varphi_{sf}(x)$  of the device and the depletion region near the tunnel junctions under the given gate and drain bias, two independent coordinates are established.

(b) Modeling results of  $\varphi_{sf}(x)$  while drain bias stays at 1V as gate bias changes between -0.6V and 0.6V.

(c) Modeling results of  $\varphi_{sf}(x)$  while gate bias stays at 0V as drain bias changes from 0V to 0.8V.

#### **Ambipolar BTBT current modeling**

Based on  $\varphi_{sf}(x)$ , the energy band of source and drain junctions can be derived (Fig. 3a & b) and the tunneling width  $W_t$  is obtained for further calculation of BTBT current. Considering the tunneling of holes at the drain junction in Fig. 3(b), the lateral distance corresponding to  $\Delta \varphi = E_g/q$  is  $W_{t,D}$ , which is solved based on surface potential model (Eq. 2, 5) and expressed as Eq. 7. The beginning and ending point of the tunneling window (green shaded area) at the drain junction with minimum and maximum tunneling paths can be obtained (Eq. 8-10). Modeling of tunneling path at source junction is similar to the above discussion, which is given by Eq. 11-13.

Furthermore, the BTBT current is calculated based on the integral of tunneling generation rate  $G_{tun}$  in Kane model [11] (Eq. 14). The distribution of  $G_{tun}$  in the tunneling windows of both source and drain regions are considered. For x-direction parallel to the channel, the generation rate is dominated by the exponential term of  $W_t$ , and thus G<sub>tun</sub> in the tunneling window will decay exponentially from  $x = x_{\text{begin}}^{\min}$  (corresponding to the shortest tunneling width) to the left and right sides until the tunneling window closes, that is,  $G_{tun}(x) \approx G_{tun}^{max}$ .  $\exp(-|x - x_{\text{begin}}^{\min}|/\lambda_t)$ . For y-direction, the  $G_{\text{tun}}$  decreases with depth exponentially as  $G_{tun}(y) \approx G_{tun}^{max} \cdot \exp(-y/t_{eff})$ , where  $t_{eff}$  is effective channel thickness. Finally, the integral of the ambipolar BTBT current can be expressed as Eq. 15. The simulated results based on our proposed model are shown in Fig. 3(c)(d). There is an off-state platform when  $V_{ds}$  is small since the tunneling windows in both source and drain junctions are not open (Fig. 3c). When  $V_{ds}$  increases, the output characteristic curve will saturate at  $V_{ds}$ =1.2V as given in Fig. 3d.



Figure 3: Energy band, surface potential, and tunneling paths at the (a) source- and (b) drain-channel junctions. Modeling results and energy band of the (c) transfer and (d) output curves without considering the FE switching.

#### FeTFET model with ambipolarity and non-volatility

The FeTFET device is constructed by connecting the FE capacitor to the gate of the TFET in series (Fig. 1a). Based on the proposed surface potential model, the effects of ambipolarity on inversion/depletion layer charge and gate capacitance model are also reconsidered [9]. Further combining the proposed analytical ambipolar TFET model with dynamic Preisach model based FE capacitor in HSPICE [9], the FeTFET with both ambipolarity and ferroelectric non-volatility is established.

The results of FeTFET model are shown in Fig. 4. When applying gate voltage sweeping with relatively low amplitude, the FeTFET is operated in the non-destructive readout mode without hysteresis in  $I_{ds}$ -V<sub>G</sub> curve (Fig. 4a) since the voltage drop on the FE layer is not enough for FE polarization switching. When applying relatively high V<sub>G</sub> (Fig. 4b) that can make the FE switching, the  $I_{ds}$ -V<sub>G</sub> curve shows typical FE hysteresis with ambipolarity.



Figure 4: Modeling results of  $I_{ds}$ - $V_G$  curve with relatively (a) low and (b) high sweep amplitude showing hysteresis. (c)  $I_{ds}$ - $V_G$  curves after applying different programming pulses and the implement schematic of XNOR-operation; -(d) Truth table of FeTFET based XNOR-operation. By applying different programming pulses and then measuring  $I_{ds}$ - $V_G$  in non-destructive readout mode, the threshold voltage of FeTFET can be programmed to different states, representing different weights as shown in Fig. 4c. Only if input  $V_G$  level and stored weight are the same, the FeTFET will have a relatively high current  $I_H$ , otherwise, it is in the off-state with low current  $I_L$  (red), indicating the XNOR-operator (Fig. 4d).

### CONCLUSION

In this paper, based on the surface potential model in tunneling junction of drain and source regions, a compact model of FeTFET is established with ambipolar BTBT current under both positive and negative  $V_G$  and non-volatile modulation of FE gate stack. The XNOR operation in one FeTFET device is also simulated based on proposed model, showing its high applicability for further FeTFET-based circuit design and simulation for edge AI application.

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