INTEGRATION STRATEGY ON LOW-COST CHIP-FIRST FAN-OUT PANEL LEVEL PACKAGING

Cheng-Tar Wu, Junbo Jiang, Mengqiang Li, Chen Xiang, and Minghao Shen*
Chengdu ESWIN System IC Co., Ltd.
Chengdu, Sichuan Province, China
*Corresponding Author's Email: terry.wu@eswin.com

ABSTRACT

In the fan-out packaging (FOP), a higher lithography cost induced by the reconstituted die shift has yet been overcome, especially in the gradually increased carrier size in recent advance, e.g. panel-level-packaging (PLP). Our previous study demonstrates that with proper die shift compensation, the post-molding/grinding 3-sigma die shift value in X and Y for the whole panel with size of 510mm × 515mm are over 200um. The die shift data is collected and input into a software algorithm to synthesis a 99.8% photolithography yield within ±12um lithography overlay specification under an exposure field size that contains 4 × 4 die array (28.4mm x 28.4mm).

By confining the die shift induced by the mold flow and pre-shifting the die in consideration of the effective coefficient of thermal expansion of FOPLP, the post-molding/grinding die shift 3-sigma value in X and Y is then improved to 109um and 108um, respectively, rendering the exposure field size increasing to greater than 10 times (99.4mm x 99.4mm) than that of 4 × 4 die array, meanwhile maintain the lithography yield at a comparable level.

Keywords—FOPLP; Die shift; Lithography yield; Exposure field.

INTRODUCTION

It is well known that fan-out packaging (FOP) has better electrical and thermal performance, as well as smaller form factor. Typical FOP can be categorized into chip-first face-down (CFFD), chip-first face-up (CFFU) and chip-last face-down (CLFD). Most of commercial packages, e.g. fan-in wafer level packaging (WLP) and PBGA, can be adopted to FOP, however, the incentive in production cost is not quite obvious, especially in CF approach.

In a CF process, the critical challenge is the die shift resulted from molding process and carrier expansion [1]. Therefore, a costly step-by-step exposure correction is required to remedy the shifted die, providing a good patterning yield. Though with proper die shift compensation ease the loading of the exposure tool, the site-by-site correction is inevitable.

In this study, CFFU approach (Fig. 1) is used to reconstitute chip on a 510mm × 515mm panel followed by redistribution layer (RDL) process. Fan-out panel-level packaging (FOPLP) has a larger carrier usage ratio in comparison with FOWLP. The larger the effective area, the longer the lithography process time is anticipated. Thus, an intention to maximize the exposure field size to increase the throughput for low-cost consideration.

Here, attempts to improve the post-molding/grinding die shift during die attach process are investigated. Furthermore, a stepper is used for die position mapping followed by data transferring to a software algorithm to synthesize the atop patterning overlay and yield at different exposure field size. With the integration of the improvement in the die attach process and overlay/yield prediction, offering a low-cost strategy that is suitable for FOPLP.

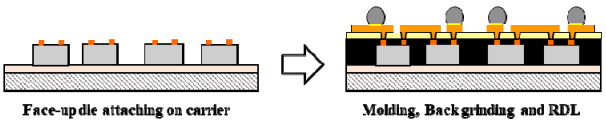


Figure 1: Schematic of chip-first face-up process

EXPERIMENTAL

Test Vehicle Chip

A bumped test vehicle (TV) chip of a package size of 7.1mm × 7.1mm was designed for the experiment. Fig. 2 (a) shows the pillar pattern of the TV. Fig. 2 (b) and 2 (c) are the alignment marks for the position mapping and overlay test, respectively.

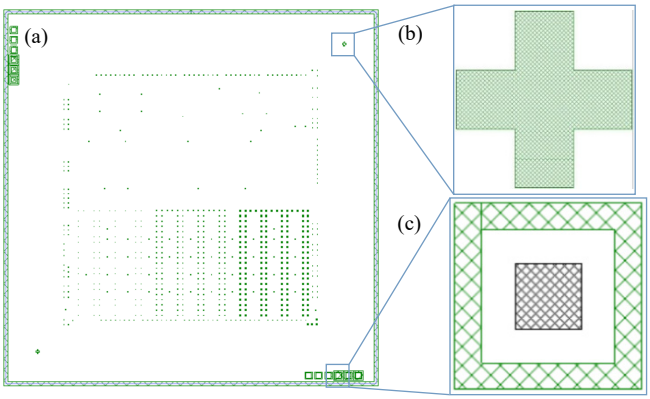


Figure 2: Test vechicle layout of (a) die pattern, (b) alignment mark for mapping, and (c) pad (green mesh)/via (grey mesh) overlay test pattern

Reconstituted Panel Fabrication

CFFU with global alignment was initially adopted for the reconstitution process. Bumped dies were transferred from a diced wafer to a bonding adhesive pre-applied glass panel with a size of 510mm × 515mm followed by a compression molding process. The reconstituted panel was consisted of 4,100 units of TV chip. A grinding process were then applied to expose the pillar pattern. Die position was then collected by measuring the alignment marks via a corrected mapping system. Since the main contribution of the die shift comes from the shrinkage of the EMC, pre-shift and enhanced local alignment were then introduced for the die shift compensation.

Mapping system for die shift measurement

A reliable mapping system is needed to provide a clear guidance for the following work on die shift compensation. To prevent tool basis, the stepper was the only mapping tool for the offset measuring.

Calibration method of mapping system was used the same approach as we reported elsewhere [2]. As seen from Fig. 3, the overlay error 3-sigma is within ±1.5μm, which is at a good level and consistent with our previous study.

The grinded panels were then fully characterized by the stepper of the die positions in each step.

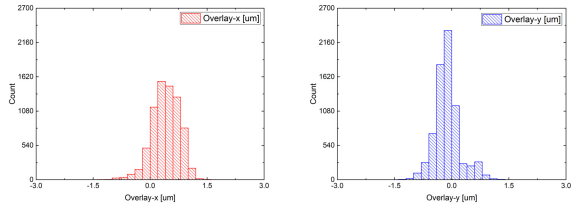


Figure 3: Overlay error with mapping and compensation from the stepper

Simulation on Exposure Field Size

A universal lithography solution for overcoming the dramatic die shift in the FOP is to expose the atop pattern by die-by-die exposure, which has been proven for a high yield, but less productivity surely. For high-volume-manufacturing (HVM), throughput and lithography overlay yield need to be considered simultaneously. Fig. 4a shows the die layout of a whole panel. The simulation of the software algorithm was carried out to guide a reasonable design for the exposure field size that matches with HVM boundaries [3]. Fig. 4b shows the schematics of three different field sizes of the 2nd layer via pattern we applied to the software algorithm, covering 1 (1 × 1), 16 (4 × 4), and 196 (14 × 14) TV chip, as shown in Fig. 4b. Site-by-site alignment was used for the simulation, synthesizing the corresponding overlay. The software algorithm was then worked out the yield in each field size.

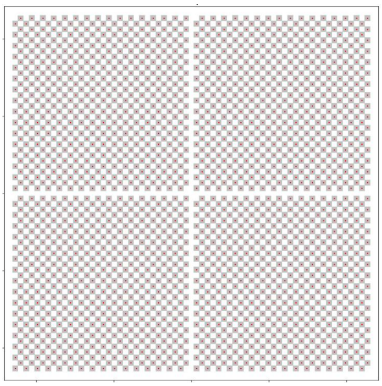
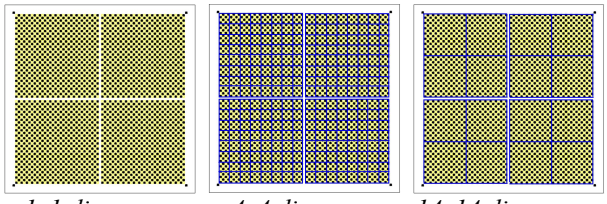


Figure 4a: Full panel die layout



1x1 die array *4x4 die array* *14x14 die array*

Figure 4b: Die layouts with designated exposure field size

RESULTS AND DISCUSSION

Die Attach Improvement in Reconstituted Process

Die shift compensation is a straightforward way to enhance the backend patterning yield in the FOP [4]. Here, few attempts were made to control the post-molding die shift in a good manner:

a) BKM: the baseline as described in the experimental that a global alignment with respect to the corner of the panel is used for die positioning.

b) Phase 1: on the basis of BKM, the effects of shrinkage/expansion of involved materials were calculated and compensated during the die attach process.

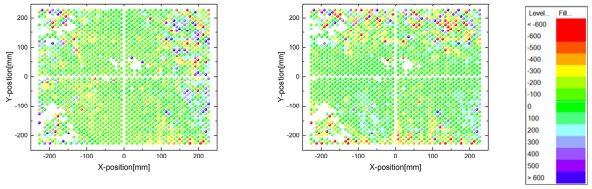
c) Phase 2: on top of the work in the phase1, a precise local alignment was added.

Table I summarizes the 3-sigma die shift in each panel at different stages. The die position was shifted dramatically away from its designated position over ±600μm in both X- and Y-direction and the θ rotation can up to 5mrad. Offset improvements to below ±190um was achieved while the mismatched of involved materials is considered. With the local alignment enhancement introduced in the phase 2, the within panel die shift was then improved to ca. ±100um, downing to one sixth of the value obtained from the BKM.

TABLE I. COMPARISON OF DIE SHIFT 3-SIGMA UNDER BKM, PHASE 1, AND PHASE 2 CONDITIONS

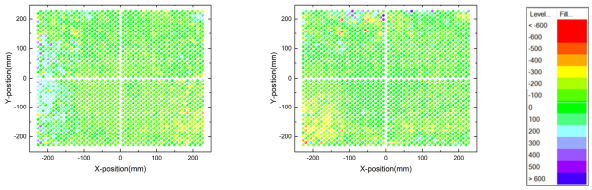
Die Attach Condition	Die Shit Performance		
	Δx (um)	*Δy (um)*	*(mrad)*
BKM	627	701	5.0
Phase 1	186	187	3.8
Phase 2	109	98	2.2

The full panel die shift in each phase is illustrated in Fig. 5. Fig. 5a, the BKM, shows the largest shift, concentrating at outer zone of the panel. This is because the center of the coordinate system for the reconstitution process was referred by the corner of a panel. The farther from the center, the larger shift impacted by the expansion of the carrier and the shrinkage of the molding compound was observed. Phase 1 has offset the contribution of material expansion/shrinkage for the process, reducing most shift, nevertheless near edge die gives a comparatively large shift, as shown in Fig. 5b. Local alignment further confined die shift, giving evenly distributed dies on the panel in the phase 2 (Fig 5c).



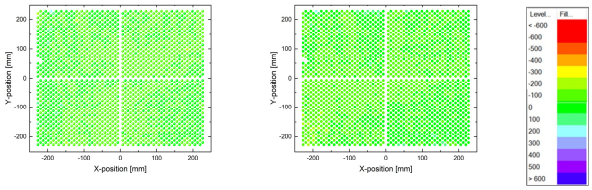
Δx (um) *Δy (um)*

Figure 5a: Die shift performance without compensation



Δx (um) *Δy (um)*

Figure 5b: Die shift with compensation in phase 1



Δx (um) *Δy (um)*

Figure 5c: Die shift with compensation in phase 2

Lithography Overlay Prediction

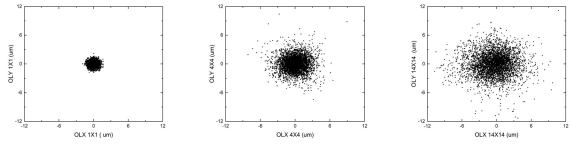
Table II summarizes the 3-sigma overlay at different phases while different exposure field sizes were implemented for yield prediction [5]. Both phase 1 and phase 2 did a great improvement in respect of overlay on a greater die array.

Comparing with the 4 × 4 die array exposing, the overlay obtained over phase 2 was improved to ca. 1.5 times than that of phase 1. Even on a larger exposing field size of 14 × 14 die array at the phase 2, the overlay in X and Y are 7.82um and 7.24um, respectively, which can be controlled at the same level of phase 1.

TABLE II. COMPARISON OF OVERLAY ERROR 3-SIGMA (MICRON) OVER 1 × 1, 4 × 4, AND 14 × 14 DIE ARRAY ON STEPPER, WITH CONTINUOUS IMPROVEMENT IN DIE ATTACH PROCESS

Overlay Error- Standard Deviation (um)						
Die Array	*BKM*		*Phase 1*		*Phase 2*	
	X	*Y*	*X*	*Y*	*X*	*Y*
1 × 1	1.49	1.52	1.52	1.49	1.51	1.51
4 × 4	27.68	23.61	**7.52**	**7.24**	4.80	4.79
14 × 14	37.25	36.35	12.35	13.47	**7.82**	**7.24**

We further analyze the combination of different field sizes in phase 2 as shown in Fig. 6, expressing that the larger the exposure field size, the less stable of lithography overlay is obtained. It is, however, a reasonable overlay standard needs to be set for evaluating the yield of lithography overlay efficiently.



1×1 *4×4* *14×14*

Figure 6: Scatter maps of overlay error with different exposure field sizes in phase 2

Lithography Yield and Throughput Improvement

Overlay yields are highly correlated with overlay specification as well as the exposure field size. Table III summarizes the prediction of the lithography overlay yields corresponding to different die array exposure fields and overlay specifications.

For HVM, the industrial overlay specification and yield are ±15μm and 99.5%, respectively. A tighten spec of smaller than ±12μm was used in this paper. It is obvious that die-by-die exposure can provide 100% yield even the tightest overlay spec is applied, which has the greatest number of exposure shots and is also time-consuming.

A 99.8% yield can be synthesized under a larger exposure field size of 4 × 4 die array when materials effect was well considered for die shift compensation, providing a practical result for HVM, but again, costly. A favorable result is obtained from the phase 2, the field size is increased to 14 × 14 die array (99.4mm × 99.4mm), meanwhile maintain the yield at 99.9% under the ±12μm overlay spec. This promising result suggests that we can expose with the fewest shots. Consequently, the

throughput can be greatly improved to 12.2 times than that of 1 × 1 exposing, as seen in Fig. 7.

TABLE III. OVERLAY YIELD PREDICTION UNDER DIFFERENT EXPOSURE FIELDS

Overlay Yield with Various Exposure Field (%)				
Conditions	***Die Array***	***±3μm***	***±6μm***	***±12μm***
BKM	1 × 1	**100.0%**	**100.0%**	**100.0%**
	4 × 4	5.7%	29.0%	73.6%
	14 × 14	1.4%	11.4%	42.9%
Phase 1	1 × 1	**100.0%**	**100.0%**	**100.0%**
	4 × 4	52.5%	92.7%	**99.8%**
	14 × 14	21.8%	64.5%	97.7%
Phase 2	1 × 1	**100.0%**	**100.0%**	**100.0%**
	4 × 4	82.8%	99.3%	**100.0%**
	14 × 14	53.7%	93.0%	**99.9%**

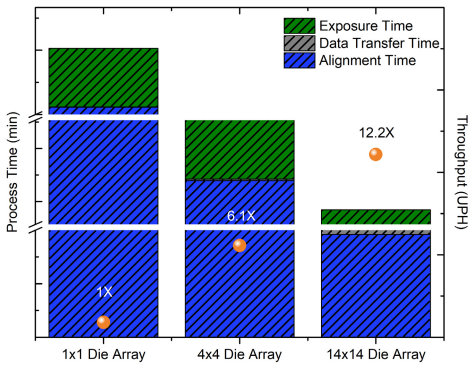


Figure 7: Throughput under different exposure field sizes, whole process time is considered

CONCLUSION

An integration of die reconstitution, die position mapping and exposure field size simulation on CF FOPLP has been demonstrated. The continuous improvement in the reconstitution process has successfully compensated the die shift that induced by compression molding, giving evenly distributed dies over the entire panel. Moreover, the post-molding die shift is reduced significantly to ca. a hundred microns level within a 510mm × 515mm panel.

The software algorithm was also presented to simulate the lithography overlay and yield over corresponding exposure field sizes, preventing massively rework in multilayers lithography process. In addition to these, an optimized field size can be predicted and implemented that helps to improve the throughput greatly. This approach has the potential for lower cost of ownership and superimpose the inherent advantage of higher carrier usage ratio of panel, offering a promising strategy on low-cost FOPLP production.

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