THE EFFECT OF STI DIVOT ON PLANNER LOGIC DEVICE PERFORMANCE STUDY

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ABSTRACT

In this paper, different etching methods and adjustments of the etching amount have been tried and the effect of increased depth of the STI divot on the performance of the planar logic device in the STI process was studied. The results showed that under the same etching amount on a blank wafer, wet etching would obtain larger divot features than dry etching. This paper also studied the relation is about 0.78 between blank wafer etching amount and structure wafer divot depth on the 28nm logic process. There are 3~5% performance improvement by STI divot increased around 30A of Core device nominal P and SRAM PU was been shown on 28nm HKMG platform. And the GOI TDDB of PMOS devices got significant improvement.

INTRODUCTION

The size of semiconductor chips continues to shrink, but still keeps its high performance and low power consumption. It makes the semiconductor process continue to challenge the limits, so the process parameters of each stage also need to be more finely optimized and adjusted for extreme performance improvement. The focus of this article is the optimization of 28nm HKMG STI divot features for device performance improvement.

As well-known, STI divot will induce some side effects, such as junction leakage, the poly residue, inverse-narrow-width effect, and double-humped I-V curve…etc. [1]-[5].

There are many discussions to reduce STI divot [6][7], but the STI divot is also increasing the short-channel area between poly gate and Si surface, and the advantages of improving channel performance are rarely mentioned [8]. This paper will discuss the effect of etching methods for the STI divot feature and the impact of divot depth on the performance of 28m HKMG logic devices.

EXPERIMENTS

To study the effect of gate1 oxide(OX) pre-clean process and oxide loss on STI divot, four split conditions were designed as shown in TABLE I. Split 0 represented the DRY etching and WET etching processes. Split1 changed DRY etching to WET etching process while keeping the oxide loss amount the same. Split2 and Split3 increased the WET etching oxide loss amount separately by about 20A and 50A compared to Split1. The experiments were processed on a 28nm HKMG pattern wafer.

TABLE I. STI DIVOT SPLIT CONDITIONS

Condition	*Dry etching OX loss (A)*	*Wet etching OX loss (A)*	*Divot (A)*	*Divot-D0 (A)*
Split0	L1	L2	D0	0
Split1	0	L1+L2	D1	24
Split2	0	L1+L2+20	D2	30
Split3	0	L1+L2+50	D3	63

RESULTS

Physic Comparing by Etching Splits

Figure1 shows the STI divot TEM results of the different gate1 oxide pre-clean process split. The comparison of Figure1 (a)~(b) shows that under the same etching amount on a blank wafer, wet etching obtained 24A larger divot than dry etching. Figure1 (b)~(d) shows that the STI divot increased by the WET etching oxide loss amount increased, and the ratio of the divot depth increase by the wet etching amount of blank wafer was about 0.78.

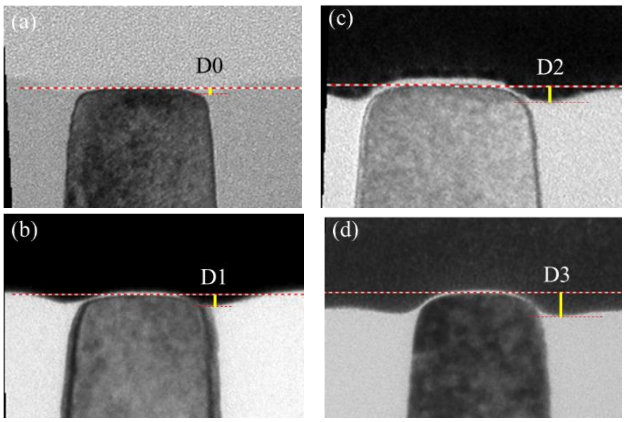


Figure 1: STI divot TEM results: (a) Split0 (b) Split1 (c) Split2 (d) Split3

Core Device by Etching Splits

Figure2 shows the nominal core device (poly length 0.03um) performance of different STI divot split on 28HKMG pattern wafer. When STI divot increased around 30A, then PMOS performance increased 3~5%, while NMOS device performance kept the same.

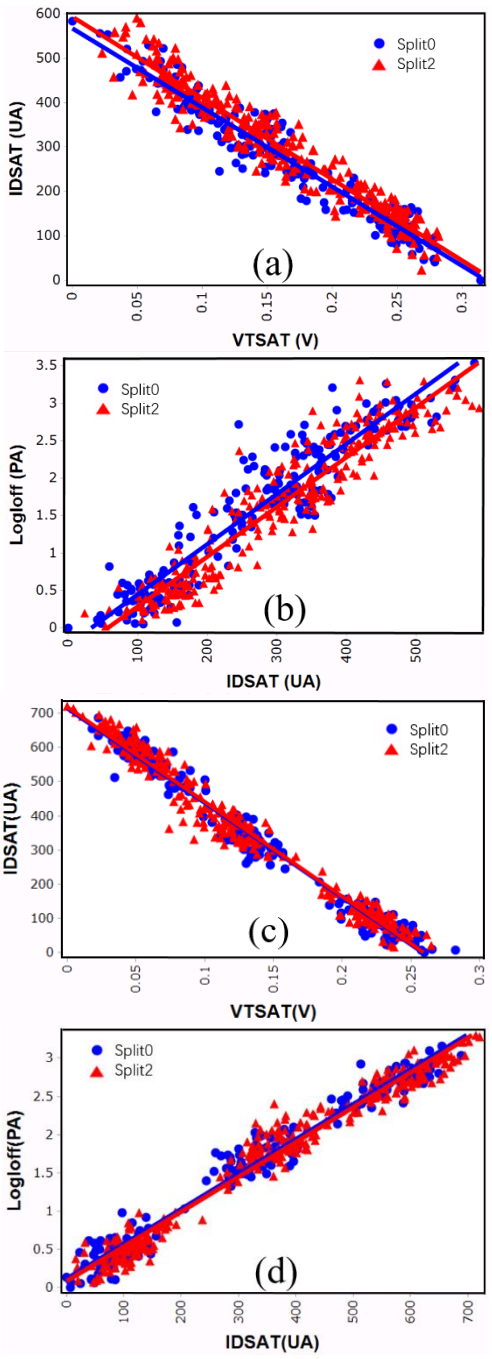
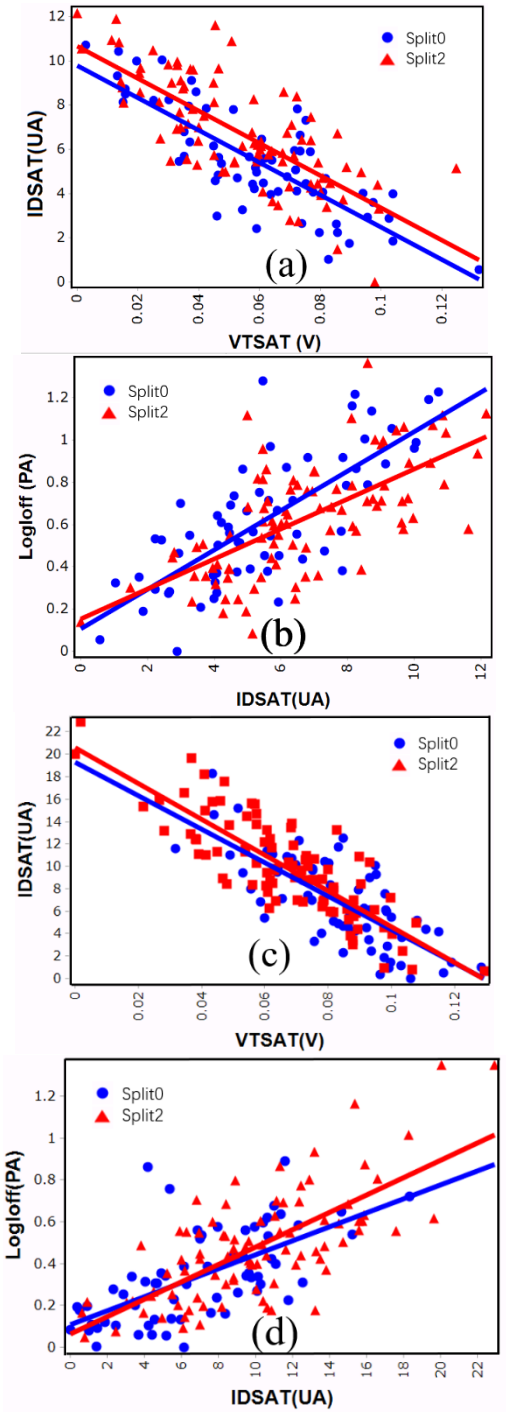


Figure2: Core device performance of different STI divot split: (a) nominal P Vt vs. Id; (b) nominal P Id vs. Ioff; (c) nominal N Vt vs. Id; (d) nominal N Id vs. Ioff.

SRAM Device by Etching Splits

SRAM performance shows the same trend as a core device. The results were shown in Figure3, SRAM PU Vt-Id and Id-Ioff performance gained 3~5%, while PD/PG performance kept the same.



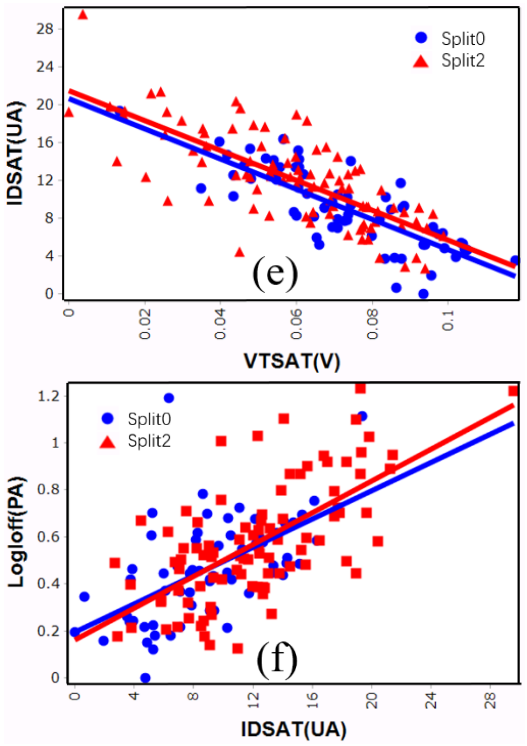


Figure3: SRAM performance of different STI divot split: (a) PU Vt vs. Id; (b) PU Id vs. Ioff; (c) PD Vt vs. Id; (d) PD Id vs. Ioff; (e) PG Vt vs. Id; (f) PG Id vs. Ioff;

Reliability by Etching Splits

Figure4 shows the PMOS GOI TDDB of different STI divot split on 28HKMG. It shows that the T63% of Split1/Split2/Split3 were significantly improved than split0. The improvement of PMOS GOI TDDB was getting obvious when the STI divot depth was highly increased.

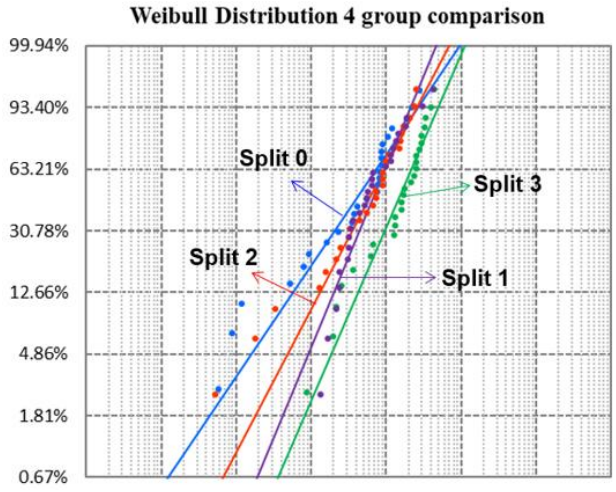


Figure4: PMOS GOI TDDB of different STI divot split

CONCLUSIONS

The effect of STI divot on the planner logic device performance was studied in this paper. The results showed that under the same etching amount of blank wafer, wet etching would obtain larger divot depth than dry etching. For a planar 28nm logic process, the ratio of the divot depth increase by the wet etching amount on a blank wafer was about 0.78. In the 28HKMG logic process devices, when STI divot increased around 30A, PMOS SRAM PU performance also increases 3-5% higher, NMOS device performance kept the same, and the GOI TDDB of PMOS devices was significantly improved. The model was STI divot increased the short-channel area between poly gate and Si surface. It is slightly like a FinFET structure.

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