STITCHING PROCESS DEVELOPMENT ON 300MM WAFER CMOS BEOL FOR HIGH PERFORMANCE CHIP APPLICATION

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ABSTRACT

In this work, stitching process was developed on 300mm wafer CMOS BEOL for high performance chip application. Different stitching pattern and process was designed and implemented to verify the process performance, including different pattern overlap length, hammerhead dimensions, etc. Based on process data, optimized process condition was obtained to achieve better process performance.

INTRODUCTION

With CMOS technology developing and consumer market growing, more and more high-end applications for large chip size are emerging, such as large chip for X-ray image sensor, wafer-size CMOS-Image-Sensor or AI chip, etc. [1-3] As known to all, chip size should be smaller than shot size of the litho tool, which is commonly 33mm X 26mm. To develop a chip beyond the size limitation, stitching is a promising choice [4-6]. By establishing electrical interconnections between neighboring shots, chips in different shot can be merged into a bigger one.

In this work, stitching process was developed on 300mm wafer CMOS BEOL. Different stitching patterns and process were designed and implemented to evaluate the process performance. The profile and process window of the stitching patterns was compared. Based on the process data, optimized process condition, especially the design rule of stitching line ends, was obtained to achieve better process performance.

EXPERIMENTS

To reduce the cost and achieve higher yield, the chip stitching was realized on 4X Cu BEOL interconnect layer of 55nm technology node, whose line/space design rule is 0.36um/0.36um. The film stack is as follows: substrate \ SiO_2-3500A \ SiN-1000A \ SiO_2-9500A \ SiON-700A \ photoresist-12000A, in which the SiON film was used as an anti-reflection layer.

The stitching patterns were designed on mask with different critical dimension (CD). As shown in Fig.1, "a" is min non-stitching line CD, "b" is the half of the hammerhead enlarged CD, "c" is the hammerhead length, "d" is the stitching pattern overlapped CD, "e" is the space between two adjacent hammerhead, "f" is the space between two adjacent non-stitching lines with hammerhead on the line end. And "c" is fixed at 0.36um, and "d" is fixed at 0.12um and can be adjusted by tuning the overlap area of litho process condition. In the experiment, different stitching patterns were put on the same mask to compare the performance. Neighboring dies were exposed with separate and precise position control by the scanner. And they were exposed using the same energy dose at which 360nm dense lines outside the stitching area were on the target, so that lines without stitching could be used as reference.

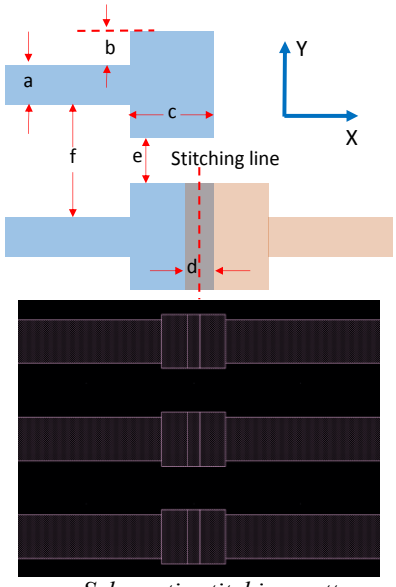

Figure. 1: Schematic stitching pattern with critical dimension (upper) and designed stitching pattern layout (lower)

All the process was developed on 300mm wafer BEOL LAB of Shanghai ICR&D Center. The litho tool used is ASML XT860M scanner. Following the litho process, dry etch and wet clean was conducted on the wafers. Both after-development inspection (ADI) and after-etch inspection (AEI) were applied to check the stitching process performance with CD-SEM Hitachi CG4000.

RESULTS AND DISCUSSION

To achieve higher metal wire density, smaller hammerhead Line/Space is required. Thus the stitching of dense lines without hammerhead was checked first, in which line/space = 0.36um/0.36um, same as the original design rule. The patterns with different overlap length d along the X direction were exposed and checked with a rotation of 90 °. As shown in Fig.2a, when d was set to zero,

the trench CDs around the stitching line were greatly narrowed, accompanied with rising risk of bridging problem. And as can be seen in Fig.2b-2d, the stitched trench CDs were enlarged with d increasing, which in the opposite will add to the possibility of breaking resist lines. Both of the risks should be avoided in the design and process. As a result, it is necessary to have a control SPEC for the overlap length d to achieve a smooth and stable profile.

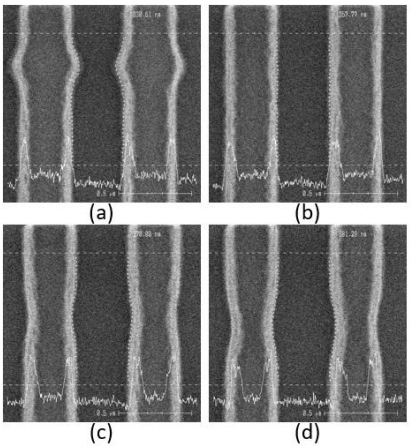

Figure. 2: ADI photos of stitched patterns without hammerhead and with different overlap d: (a) d=0; (b) d=120nm; (c) d=240nm; (d) d=360nm

In order to check the process window, above processes were repeated with an overlay of 40nm in the Y direction. As can be seen in Fig.3, the lower part of the patterns were slightly shifted rightward and the CDs around the stitching line were affected.

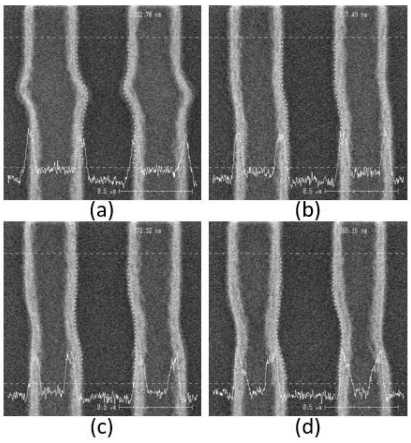

Figure.3: ADI photos of stitching patterns without hammerhead, but with an extra Y-direction overlay of 40nm and different overlap d: (a) d=0; (b) d=120nm; (c) d=240nm; (d) d=360nm

The minimum CDs of the photoresist lines and trenches were measured and plotted in Fig.4, and a 330nm red line was plotted as CD SPEC for both line and space, below which risk of bridging problem will raise. As can be seen in the figure, the allowed overlap d was limited from about 90 to 180nm, and only about 40nm process window can be obtained when setting 135nm as the optimized overlap d value.

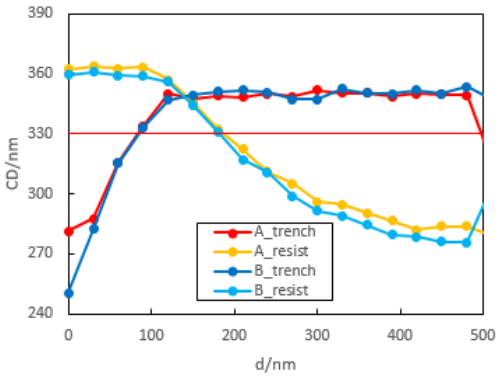

Figure.4: Minimum resist line and trench ADI CDs with different d: "A" was for patterns without overlay in Y-direction and "B" was for patterns with a 40nm overlay in Y-direction

However, 40nm overlay tolerance might not be sufficient because of increasing BEOL layer number and related process variations. Thus stitching patterns with different hammerhead dimension @ fixed a =0.36um was checked, which was shown in Fig.5. Compared with the patterns without hammerhead, stitched lines with widened hammerheads and space had robust CD performance. For the dense lines with hammerhead line/space = 0.4um/0.4um, process window of overlap d was ranging from 60nm to 500nm, and was much larger than that of the patterns without hammerhead. Further increasing hammerhead dimension to 0.45um/0.45um, the process window and performance will be even better, but at the cost of reducing metal wire density.

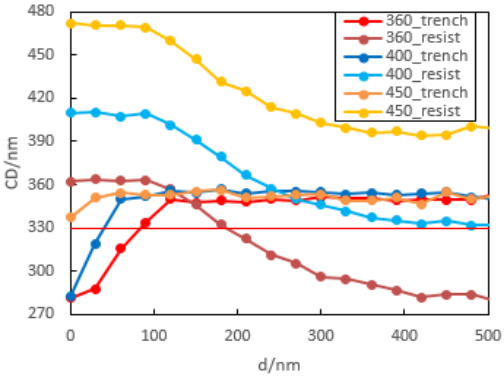

Figure.5: Minimum resist line and trench ADI CDs of different hammerhead width b and overlap d

Based on above ADI data, patterns with hammerhead of line/space = 0.4um/0.4um will be a practical choice for

stitching process of 55nm 4X BEOL interconnect layer. The stitched patterns are expected to endure certain CD variance and positioning mismatch either radially or tangentially, as long as there is a pre-defined overlap of more than 100nm.

Subsequently, the wafers proceeded to the etch process. The AEI was checked and part of the results were shown in Fig.6. & Fig.7 in comparison to the ADI photos. As can be seen in these figures, the resist patterns were successfully transferred downward and no extra defects were found. The AEI CDs were close to the ADI CDs except for a small etch bias, which could be covered by the enlarged process window using a hammerhead of 0.4um/0.4um.

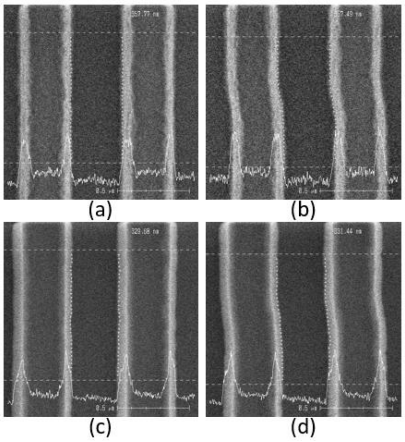

Figure.6: photos of 0.36um/0.36um stitched patterns without hammerheads: (a) ADI without Y-direction overlay; (b) ADI with an extra Y-direction overlay of 40nm; (c) AEI without Y-direction overlay; (d) AEI with an extra Y-direction overlay of 40nm

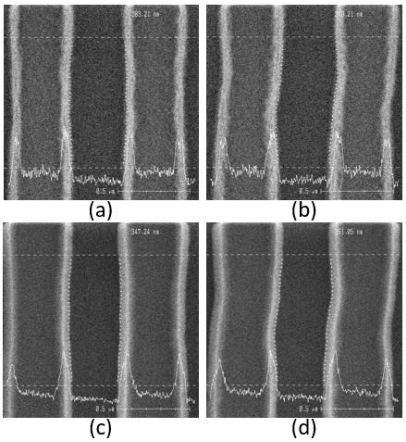

Figure.7: photos of stitched patterns with hammerheads of 0.4um/0.4um: (a) ADI without Y-direction overlay; (b) ADI with an extra Y-direction overlay of 40nm; (c) AEI without Y-direction overlay; (d) AEI with an extra Y-direction overlay of 40nm

Based on the above ADI and AEI data, stitching with hammerhead of line/space = 0.4um/0.4um and an overlap of larger than 100nm was tested to be robust in the 55nm BEOL process.

CONCLUSION

In this work, stitching process was developed on 4X BEOL interconnect layer of 55nm technology node. Patterns with different hammerhead size and overlap dimension was designed and evaluated. Based on the measured data, for dense patterns of line/space = 0.36um/0.36um, the stitching process will require a hammerhead line/space = 0.4um/0.4um.

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