FLICKER NOISE CHARACTERIZATION OF LDMOS IN FINFET TECHNOLOGY

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ABSTRACT

The flicker noise (1/f noise) behavior of FinFET LDMOS (Lateral Double-diffused MOS) transistor varies significantly from that of a conventional MOS transistor because of the extended drain region in LDMOS. Therefore, through an investigation of a 14 nm FinFET LDMOS, two distinct phenomena were discovered, discussed and first reported in this paper. Firstly, the trend of the Sid vs. Vd (drain voltage) curves was studied. The Sid vs. Vd curves exhibited an increase with drain voltage at relatively low drain voltage, then followed by a significant drop once the drain voltage reached a certain value. Space Charge Modulation (SCM) and hot spot formation theories were employed to interpret the mechanism behind this trend and this trend was linked to Quasi-saturation (QS) effect in LDMOS. Secondly, the unparalleled Sid vs. Frequency curves due to the existence of the extended drain in the LDMOS were studied. On the basis of this finding, a new BSIM-CMG LDMOS subcircuit model was proposed, which consisted a MOS transistor and a terminal voltage dependent resistor. SPICE simulation results revealed that this subcircuit model was able to accurately describe the noise behavior of the FinFET LDMOS and could be applied to tremendous fields where LDMOS plays a role.

INTRODUCTION

LDMOS, by virtue of its advantages including its compatibility with standard CMOS processing and its capability to withstand high drain voltage, has been intensively used in a vast of fields. It could be served as a crucial part in smart power devices, I/O devices, power amplifiers and HV drivers, etc. [1-2] Moreover, with the rise of electric vehicles in recent years, the prosperous applications of LDMOS in power management chips in the near future is promising.

Among all properties of interest, flicker noise property is vital for LDMOS because flicker noise constitutes a large portion from low to moderate frequencies, thus determining the performance of LDMOS in actual circuits and putting limits to the dynamic range of a device, especially in digital circuits. Some published literatures on the flicker noise behavior of LDMOS focused mainly on LDMOS with large channel length [3-4] and the flicker noise behavior of FinFET LDMOS in advanced technology node has never been reported. Besides, FinFET LDMOS has dramatic changes both in channel length and structure. Therefore, it is worthwhile to investigate the flicker noise behavior of FinFET LDMOS. In the present work, a comprehensive analysis of the Sid vs drain voltage and Sid vs. Frequency curves was carried out. In addition, a BSIM-CMG subcircuit model was proposed to simulate the flicker noise phenomena found in FinFET LDMOS, to provide an accurate model support in IC industry.

DEVICE AND EXPERIMENT

The device used in this study was an 14 nm n-type FinFET LDMOS, manufactured in SMIC through a series of delicate processes: 1) fin process to form fin structure; 2) poly process to form poly gate; 3) EPI process for channel stress engineering; 4) high-k metal gate process to remove poly gate and deposit metal layers; 5) middle end of line (MEOL) and back end of line (BEOL) processes. The cross-section schematic of the LDMOS is shown in Fig.1. Similar to conventional MOS transistor, four terminals - bulk, source, gate and drain, could be easily identified, while the channel region features gradient dopant concentration and is separated into three parts – channel, drift region and drift extension region. Shallow trench isolation (STI) sat in NWell was carried out during fin loop.

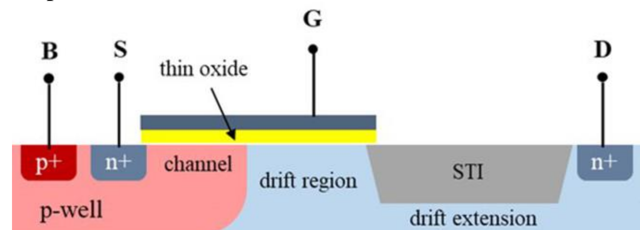

Figure 1: Schematic showing the cross-section of an 14 nm n-type FinFET LDMOS manufactured in SMIC

For flicker noise detection, measurements were performed on ProPlus 9812DX low frequency noise characterization system. Sid spectral density vs. Frequency curves were measured with frequency ranging from 5 to 100k Hz. Subsequently, flicker noise values at certain frequency were extracted from these measured noise spectrum curves for further Sid vs. Vd trend analysis

with drain voltage varying from 0.1 to 5 V.

RESULT AND DISCUSSION

The relationship between flicker noise and drain voltage was investigated as can be seen from the Sid vs. Vd curves shown in Fig. 2. Sid increases with drain voltage and this trend is typical in MOSFET transistor. However, once drain voltage reaches around 2 - 3 V, a sharp drop in Sid can be detected and this is valid over a large frequency range from 100 to 100k Hz, as shown in Fig. 2(a) – (d). Despite the physical mechanism of flicker noise is not yet fully understood, it is generally believed that the capture and emission of electrons by interface traps at the Si-SiO_2 interface plays an important role. [5] Therefore, the structural difference between LDMOS (extended drain) and MOS transistor is speculated to cause changes in trapping/de-trapping and accounts for the Sid vs. Vd trend found in LDMOS. The following discussions will focus on this issue in more detail.

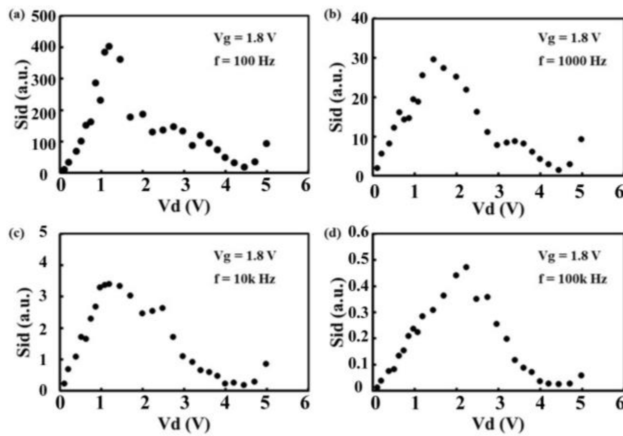

Figure 2: Sid vs. Vd curves measured at 1.8 V gate voltage over a frequency range from 100 to 100k Hz.

Initially, LDMOS works in the linear region when drain voltage is low as shown in the Id-Vd curve (Fig. 3). In this stage, noise behavior is quite similar to MOS transistor. Subsequently, with the increasing of drain voltage, the transistor gradually enters into quasi-saturation state and the carriers in the channel and extended drift region have undergo Space Charge Modulation (SCM, also called Kirk Effect). [6-7] After SCM, the electrical field in LDMOS at channel end and drain end has experienced opposite changes. At drain end, the electrical field soars with drain voltage and forms a hot spot, while slightly decreases at the channel end. Moreover, the electrical field at the channel region shifts deeper into the LDMOS from its surface. [8] As a consequence, current path in the FinFET LDMOS deviates from the surface, hindering the trapping/de-trapping process happened close to the Si-SiO_2 surface. Hence, Sid vs. Vd curve drops after SCM.

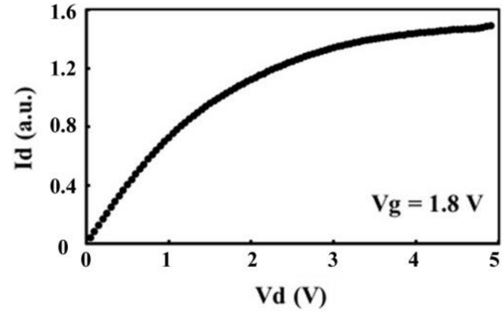

Figure 3: Id-Vd curve measured at a gate voltge of 1.8 V

The influence of SCM could be further verified by the phenomenon found in a FinFET LDMOS reliability study. In another ongoing research on the Hot Carrier Instability (HCI) effect of FinFET LDMOS, it is shown that the threshold voltage degrades less under the stress condition with SCM (~2.2 mV) compared to vt degredation under the stress condition without SCM (~9.6 mV) (data not included in this paper). Since HCI effect depicts the process that carriers gaining high kinetic energies in the lateral electrical field inject into gate oxide and cause charge trapping and interface states and this effect could be linked with SCM in LDMOS [9]. It is reasonable to deduce that the alleviation of HCI effect due to SCM will lead to the dropping trend in Sid vs. Vd curves.

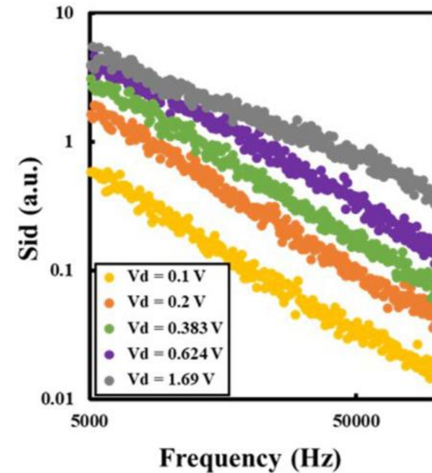

Figure 4: Sid vs. Frequency curves measured at a series of drain voltages with Vg = 1.8 V

The Sid vs. Frequency curves shown in Fig. 4 were measured at a gate voltage of 1.8 V with drain voltage ranging from 0.1 to 1.7 V. In general, the Sid vs. Frequency curves (in log-log scale) follow $(1/f)^n$ behavior as the name 1/f noise indicated. In conventional MOS transistors, the frequency exponent n is typically in the range of 0.8 to 1.2 [10], and terminal bias barely has any impact on the value of n, which results in a group of

paralleled curves. However, in FinFET LDMOS, the Sid vs. Frequency curves exhibited unparalleled trend with the increase of drain voltage as can be seen from Fig. 4, which explicitly indicates that n is dependent on drain voltage. n value drops from 1.14 down to around 0.77 with increasing Vd (from 0.1 to ~1.7 V). Considering the structural difference between LDMOS and MOS, the resistance of the extend drain in the LDMOS due to non-homogeneous doping inevitably has an impact on the 1/f noise.

On this basis, the flicker noise behavior of FinFET LDMOS could be expressed as a linear superposition of a MOS transistor and a terminal voltage controlled resistor as shown in Fig. 5(a). With BSIM-CMG model, which is the most widely used in FinFET technology, using a subcircuit model including MOS and voltage-dependent resistor, we have successfully reproduced the drops in the Sid vs. Vd curves. As in Fig. 5 (b)-(d), SPICE simulation data has shown that the newly proposed subcircuit model is able to accurately describe the Sid vs. Vd curves over a wide frequency range from 1000 to 100k Hz.

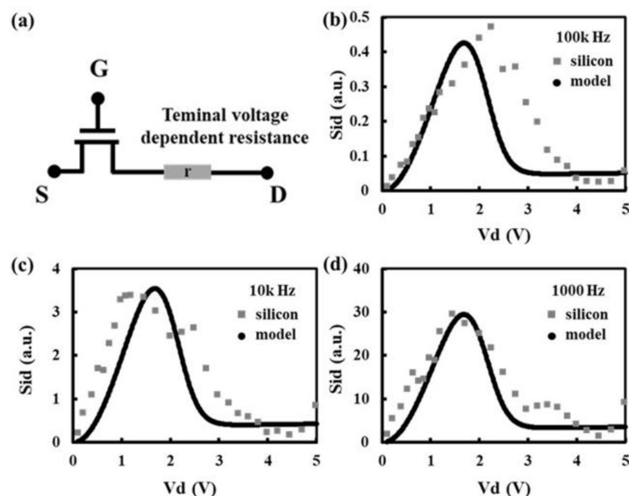

Figure 5: (a) Schematic of FinFET LDMOS consists a MOS transistor and a terminal voltage dependent resistor for FinFET modeling; (b)-(d) Sid vs. Vd curves simulated with the proposed subcircuit model at 100k, 10k and 1000 Hz, respectively.

CONCLUSION

In this paper, the flicker noise behavior of a 14 nm FinFET LDMOS was investigated through a profound discussion of the Sid vs. Vd and Sid vs. Frequency curves. A decrease trend was found in the Sid vs. Vd curves, and this trend was explained with space charge modulation and hot spot formation theories. With the increasing of drain voltage, LDMOS gradually enters quasi-saturation state and SCM happens. In this state, the corresponding electrical field in LDMOS shifts deeper in to the device, blocking the trapping/de-trapping process near the surface, thus leading to Sid drop. In the Sid vs. Frequency study, the unparalleled Sid vs. Frequency curves led us to realize the unneglectable function of the extended drain. Accordingly, a BSIM-CMG subcircuit model consisting a MOS transistor and a terminal voltage dependent resistor was proposed in order to simulate the unique flicker noise phenomena in FinFET LDMOS. The subcircuit model has proven to be accurate compared to primary silicon data from low to moderate frequencies, which could potentially be used in LDMOS related IC designs.

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