Peeling Defect Studying with N2/H2 Plasma during Carbon-based Recess Etch

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Abstract

N_2/H_2 plasmas are often adopted for controllable etching of C-based materials, such as for etching back end of line (BEOL) tri-layer resist. In this paper, N_2/H_2 chemistry has been used for a spin-on carbon (SOC) recess application in a Lam capacitively coupled plasma (CCP) etch system. Peeling defects are more problematic for this recess etch than the traditional tri-layer carbon etch due to the Si-based byproducts that form readily on SiO_2 in N_2/H_2 plasmas. Here, we report on the important role N_2 plays in this process space and describe two methods to mitigate the peeling defect mode for this application.

Keywords— N_2/H_2 carbon based etch; Si-based byproduct; Peeling Defect; O2 plasma-based carbon etch

Introduction

SOC has been widely used in BEOL etching as a mask material [1] because of its good gap-fill and planarization properties. For a via-first, dual-damascene process, to obtain a flat SOC surface, it is common to use a Dep-Etch-Dep process, with two steps of SOC dep separated by an SOC recess etch to smooth the topography and surface roughness following the first deposition, as shown in Fig.1.

N_2/H_2 has often been used to etch low-K materials, such as SiCOH [2]. N_2/H_2 has also been used to etch SOC [3] with a higher etch rate and better ER uniformity than common alternatives. During SOC recess etch, N_2/H_2 has been used to maintain good uniformity but peeling defects have been observed when run in volume.

To mitigate this peeling defect, two methods have been studied. One is to use a CF_4/O_2-based CWAC to clean the chamber between process wafers. The other method is to use an O_2-based plasma to etch SOC, which avoids generating the peeling defects during wafer processing. Further investigation has found that N_2/H_2 plasma reacts with SiO_2 to form Si-based byproducts, which can combine with C-based polymers. This byproduct combination is more challenging to remove by N_2/H_2 plasma or pure O_2 plasma.

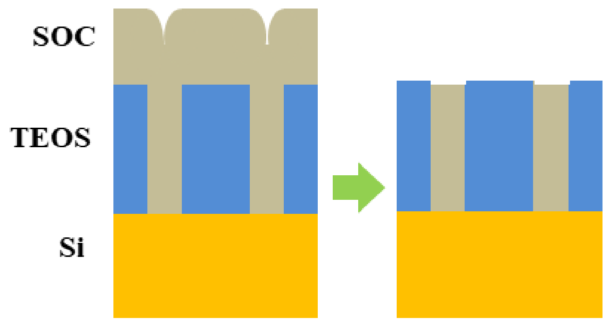

Fig.1. SOC recess etch process schematic

Experiments

This process has been developed on an industry-standard Lam CCP etch system with an endpoint algorithm to compensate for incoming process variation.

Defect scans were by Dark Field Inspection (DFI) and reviewed by scanning electronic microscopy (SEM). Elemental analysis was done by Energy Dispersive X-ray (EDX).

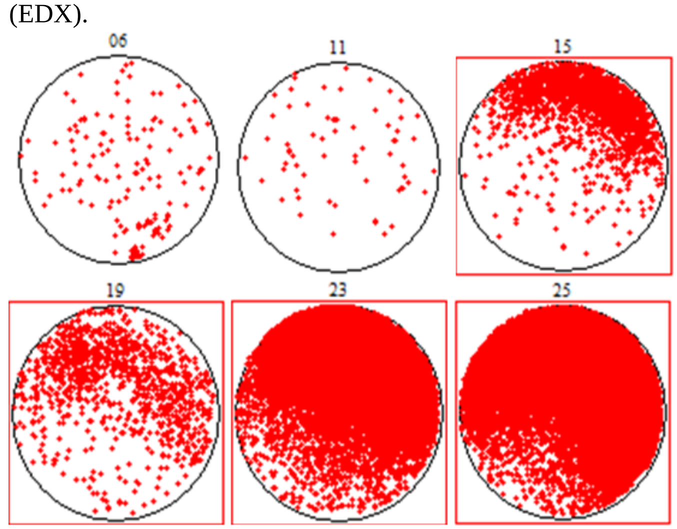

Fig.2. Defect map scanned by DFI. Defect trend worse as more wafers run.

As shown in Fig. 2, when more wafers were run, peeling defectivity trended up abruptly even within a single lot in N2/H2 plasma combining with O2 WAC. A representative

SEM review, shown in Fig. 3, shows a curled paper morphology. And the EDX elemental analysis shows composition of Si, O, and C.

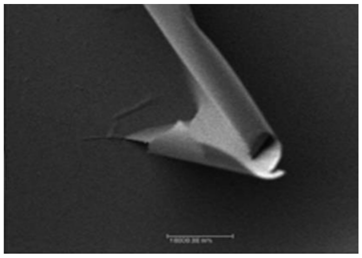

Fig.3. Peeling defect image reviewed by SEM. Element analysis shows it’s composed of Si, O and C.

Results and Discussion

Peeling defects have been found as soon as the 6th production wafer for the N_2/H_2 plasma process. An O_2-plasma waferless auto clean (WAC) has been used to clean polymer from the chamber after each wafer. Experience shows that this WAC effectively cleans pure C-based polymer, while EDX analysis shows that the polymer giving rise to peeling defects includes Si as well (Si/O/C).

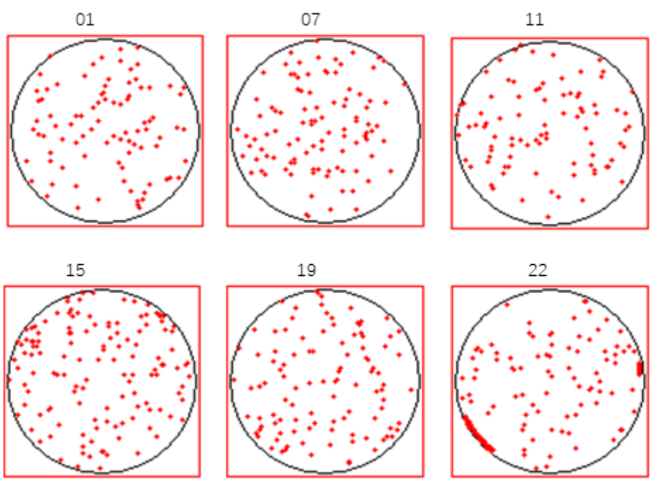

Fig4. Peeling defect is free after implementing CWAC in N2/H2 based process

Two methods have been used to solve peeling defect based on BSL condition, as summarized below:

BSL condition: N_2/H_2 plasma for SOC recess etch + O_2 WAC per wafer

Method I: N_2/H_2 plasma for SOC recess etch + O_2 WAC per wafer + CF_4/O_2 CWAC every 6 wafers

Method II: O_2 plasma for SOC recess etch + O_2 WAC per wafer

When Method I is used, the CWAC with CF_4 effectively cleans the Si-based byproduct. as Fig. 4 shows. That process proved effective in generating peeling-defect-free results in continuous-run, volume production.

Method II uses pure O_2 plasma for the process wafer etch and also demonstrates effective performance, without peeling defects under continuous run conditions. The etch rate (ER) maps in Fig. 5 show a lower SiO_2 ER for O_2 plasma than N_2/H_2 plasma, indicating that less Si-based byproduct would be formed.

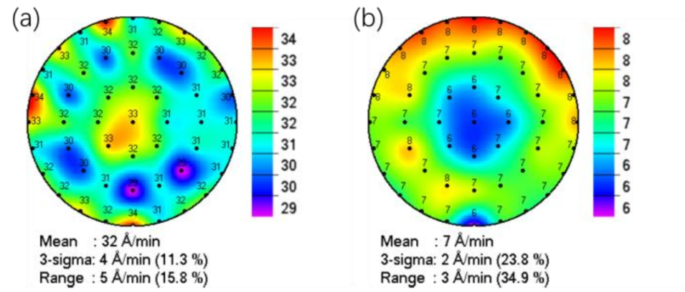

Fig. 5. Etch rate map for SiO_2. (a) N_2/H_2 plasma to etch SiO_2. (b) O_2 plasma to etch SiO_2.

Comparing BSL condition and Method II, the presence of N_2 in BSL condition is the most notable difference. Higher etch rate of SiO_2 by N_2/H_2 plasma shown in Fig. 5 generates more Si-based byproduct as well. As shown in Fig. 6, compared with Ar/H_2 plasma, N_2/H_2 plasma has higher bias voltage. We think N_2 plays an important role for the SiO_2 etch by attracting more electrons to plasma and thereby providing higher bias voltage and a concomitant increase ion bombardment to more effectively break surface chemical bonds. This results both in the higher SiO_2 etch rate and the higher incidence of Si-based byproducts in N_2/H_2 plasma.

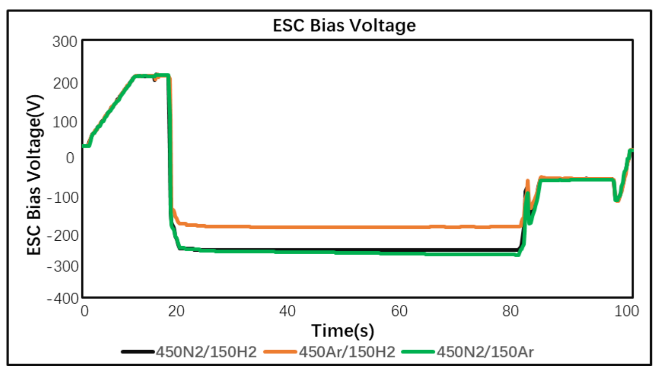

Fig. 6. Both $450N_2/150H_2$ and $450N_2/150Ar$ show comparable ESC bias voltage, and their ESC bias voltage is higher than $450Ar/150H_2$

Conclusion

In this work, both N2/H2- and O2-based plasmas were used for a SOC recess application. N2/H2 plasma etches SiO2 more readily but is also susceptible to Si-based byproducts, which can manifest as peeling defects. A CF4/O2-based CWAC was effective at cleaning the Si-based byproduct. Peeling defects could also be avoided by using the simpler and lower biased

O2-based etch chemistry.

References

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