

Si/SnS₂ VERTICAL HETEROJUNCTION TUNNELING TRANSISTOR WITH IONIC-LIQUID GATE FOR ULTRA-LOW POWER APPLICATION

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ABSTRACT

In this work, a novel Si/SnS₂ vertical heterojunction tunneling transistor (HTFET) with ionic-liquid gate is proposed and experimentally demonstrated. Si/SnS₂ tunnel junction behaves nearly-broken band alignment with effective tunneling potential height of only 0.17 eV, which is beneficial for the on-state current. Besides, due to the mature doping and contact technology of Si, excellent contacts between Si/SnS₂ and metal electrodes can be achieved. Moreover, the organic electrolyte (PEO: LiClO₄=9:1) is adopted as ionic-liquid gate stack and the electric double-layer structure formed by the anion and cation migration in the organic electrolyte can enhance the electrostatic control and optimize the subthreshold swing of the device.

Keywords—two-dimensional materials, tunneling transistor, ionic-liquid gate

INTRODUCTION

Tunneling transistors (TFETs) have attracted sustained attention due to their ultra-steep subthreshold swing (SS), ultra-low off-state currents, and no hysteresis [1][2]. Two dimensional materials have the advantages of atomic thickness, no dangling bond, sharp band edges [3]. Therefore, TFETs based on 2D materials (2D-TFET) have theoretically great potential for ultra-low power application. However, the lack of mature and controlled doping techniques for 2D materials and the high contact resistance between the metal electrode and the 2D material severely limit the application of 2D-TFETs.

In this work, we utilize Si/ SnS₂ heterojunction with near broken band alignment to construct 3D-2D vertical HTFET, which can also effectively avoid the challenges of doping and contact resistance in 2D TFETs. The fabricated device shows great potential for ultra-low power applications [4][5].

DESIGN OF 3D-2D HTFET

In this work, the Si/SnS₂ material system is adopted to construct vertical HTFET. Si/SnS₂ energy band alignment and electron affinity potential are shown in Fig. 1(a), it can be seen that the Si/SnS₂ exhibits near broken band alignment, and the effective tunneling potential height is only 0.17 eV, which can achieve high on-state tunneling current. Furthermore, Si is a conventional semiconductor material with mature doping and contact technology, which makes it an excellent source region material and can lower contact resistance with metal electrodes.

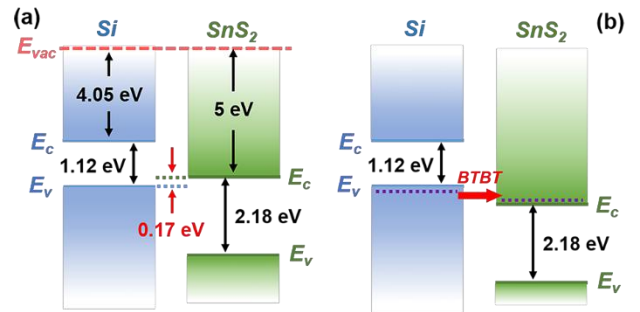


Fig. 1(a): Si/SnS₂ energy band alignment; (b): Si/SnS₂ energy band alignment when positive gate voltage is applied.

To further enhance the gate electrostatic control and optimize the SS of the device, we choose organic electrolyte as the ionic-liquid gate stack. The organic electrolyte consists of polyethylene oxide (PEO) and lithium perchlorate (LiClO₄) in a 9:1 mass ratio. The distribution of lithium and perchlorate ions in organic electrolytes is homogeneous without applying gate voltage. When the gate voltage is applied, the lithium and perchlorate ions in the organic electrolyte can be driven by the electric field to migrate to form electric double-layer structure on the surface of the channel. The electric double-layer structure has a large capacitance, which can effectively enhance the gate electrostatic

control [6]. FABRICATION OF Si/SnS₂ VERTICAL HTFET

The schematic structure and fabrication process of Si/SnS₂ vertical HTFET are shown in Figure 2. A low doping (resistivity less than 0.0015 Ω-cm) P-type <100> Si is used as the substrate. First, the natural oxide layer (SiO₂) is removed from the Si surface using HF solution, then the mechanically exfoliated SnS₂ flake is transferred onto the Si substrate. Afterwards, the SnS₂ material with appropriate thickness is deposited under the microscope by optical contrast and the surrounding region is exposed by electron beam lithography (EBL). Next, HfO₂ film with thickness of 15 nm is grown by atomic layer deposition (ALD) to isolate the contact metal of SnS₂ (not yet deposited in this step) from the Si substrate. Then, a second EBL is used to define the position of the source and drain metal electrodes. After the second EBL, the electron beam evaporation is used to deposit Ti/Au and peel off to fabricate the source and drain metal electrodes. Finally, the formulated organic electrolyte solution is dropped onto the Si and SnS₂ overlap regions to form ionic-liquid gate stack. After the above steps, the Si/SnS₂ vertical HTFET is fabricated.

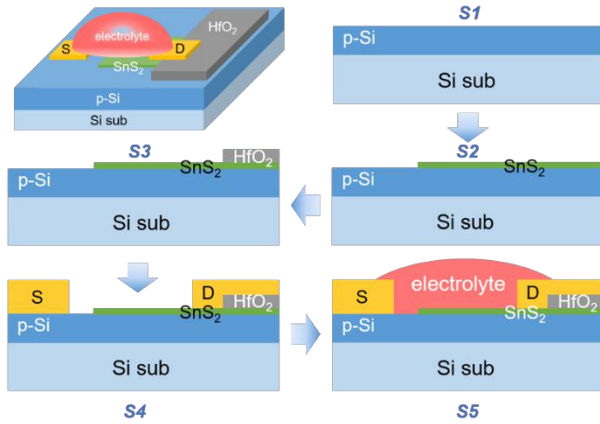


Fig. 2: Fabrication of Si/SnS₂ vertical HTFET.

ELECTRICAL PROPERTIES CHARACTERIZATION

When no gate voltage is applied, the Si/SnS₂ energy band alignment is as shown in Figure 1 (a), where the bottom of the SnS₂ conduction band is above the top of the Si valence band, the tunneling window is not formed, the device is in the off-state. When positive voltage is applied to the gate, SnS₂ is closer to the gate and is more sensitive to the change of gate voltage. Therefore, as the gate voltage increases, the energy band of SnS₂ will shift downward with respect to Si, resulting in a broken band alignment. As shown in Figure 1 (b), the electrons in the Si valence band can tunnel into the SnS₂ conduction band. Driven by electric field, electrons drift towards the drain and are eventually collected by the drain electrode,

resulting in band to band tunneling (BTBT) current.

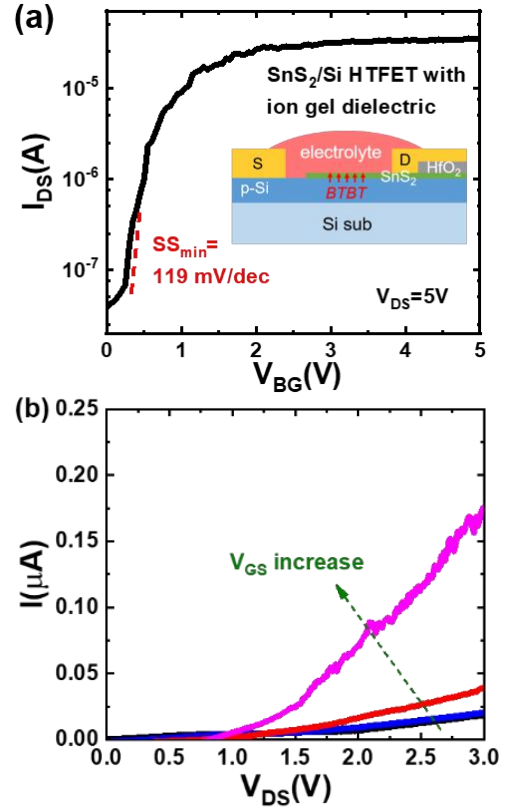


Fig. 3 (a): Transfer characteristic curve of Si/SnS₂ vertical HTFET; (b): Output characteristic curve of Si/SnS₂ vertical HTFET.

The transfer and output characteristic curves obtained from the electrical measurement are shown in Figure 3. From the figure, the fabricated Si/SnS₂ vertical HTFET can reach on-state current of 35.3 μA (Normalized current value of 5.88 μA/μm²), the current on/off ratio is 10³, and the extracted the minimum subthreshold slope SS_{min} is 119 mV/dec. Table 1 compares the on-state current of Si/SnS₂ vertical HTFET reported in this work with those of other reported 3D-2D HTFETs. It can be seen that the Si/SnS₂ vertical HTFET in this work achieves the highest on-state current, indicating its great potential for ultra-low power application.

Table 1 : On-state current of Si/SnS₂ vertical HTFET in this work and 3D-2D HTFETs reported in other works.

3D-2D HTFET	BP/InAs[7]	Ge/MoS ₂ [8]	Si/MoS ₂ [9]	This work
I _{on} (nA/μm ²)	<10 ³	274	10.1	5.88×10 ³

CONCLUSION

In this paper, we propose and fabricate a novel Si/SnS₂ vertical HTFET with ionic-liquid gate. Mature doping and contact technology of Si and nearly-broken

energy band alignment of Si/SnS₂ material system improve the on-state current of the device. Moreover, the electric double-layer structure formed by the migration of anions and cations in the organic electrolyte gate stack can also enhance the gate electrostatic control and optimize the SS. The fabricated Si/SnS₂ vertical HTFET shows the highest on-state current among 3D-2D HTFETs, showing its great potential for ultra-low power application.

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