THE EFFECTS OF POLY CORNER ETCH RESIDUE ON ADVANCED FINFET DEVICE PERFORMANCE

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ABSTRACT

In this paper, we study the effect of poly corner residue during a 5nm FinFET poly etch process using virtual fabrication. A systemic investigation was performed to understand the impact of poly corner residue on hard failure modes and device performance. Our results indicate that larger width and height residues can lead to a hard failure by creating a short between the source/drain epitaxy and the metal gate. Surprisingly, a properly-sized residue can boost device performance with a greater than 8% on-state current increase and about a 50% off-state current drop, compared with having no poly corner residue. This increase in performance is primarily due to the reduction of access resistance between the source/drain and gate during the on-state, and better gate control during the off-state. This study demonstrates that proper residue size and variation control in the poly etch process is required to balance yield and device performance.

INTRODUCTION

With continuing FinFET device process scaling, structure profiles and micro loading control become increasingly important due to their significant impact on yield and device performance [1-2]. Dummy poly profiles is an example of the importance of structure profiles, since they directly determine the FinFET gate length. A minor change in this profile will lead to a large shift in device performance, due to the narrower and narrower gate CDs at advanced nodes. Unfortunately, it has become increasingly difficult to control the dummy poly profile due to the smaller pitch and higher aspect ratios of current generation FinFET devices. Ion shadowing occurs during the gate etch process because of the high aspect ratio of gate and fin structures. This shadowing creates a poly corner residue at the corner of the fin cross poly area, and the residue can directly change the channel profile and significantly impact device yield and device performance. The impact of this poly corner residue on yield and device performance, and what residue size is acceptable, needs to be more fully investigated. In this paper, we will mimic poly corner residue behavior in the SEMulator3D® virtual fabrication platform, and systemically investigate its impact on both yield and device performance. [3].

POLY CORNER RESIDUE INVESTIGATION, MODELING AND FAILURE MODE ANALYSIS

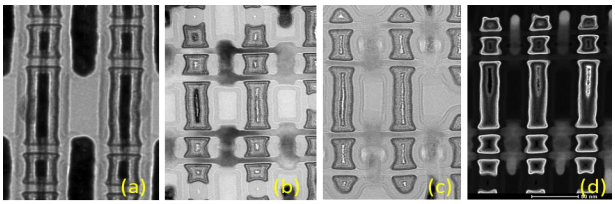

Figure 1: Gate profile at fin level, (a) 12nm, (b)/(c) 10 nm, (d) 7 nm (Courtesy from Techinsights).

Poly corner residue induced metal gate protrusion at the fin cross gate area can be found at many different FinFET nodes (Figure 1), highlighting that it is a common phenomenon during the poly etch process [4-7]. To understand poly corner residue mechanisms, limited visibility and pattern dependent etch operations must be modeled. SEMulator3D provides a novel pseudo-3D approach to pattern dependence modeling based on 2D proximity functions. The proximity functions are convoluted using a pattern-dependence mask, within a characteristic distance of a point of interest, to produce a 2D loading map to modifies the behavior of behavioral etch algorithm in the software [8].

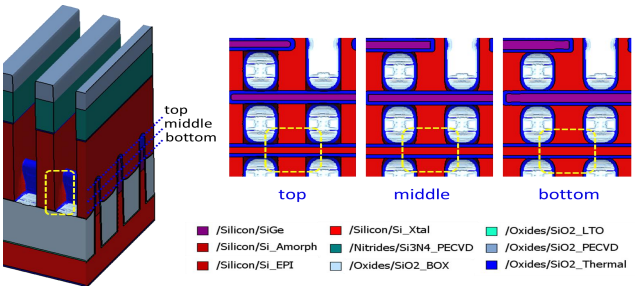

Figure 2: Fabricated 3D corner residue and its profile at different elevations.

A 5 nm virtual process flow was built in SEMulator3D to study poly residue behavior. In the flow, SRAM111 is selected as the nominal structure, with a fin CD of 6 nm, fin height of 50 nm, a source/drain Si recess depth of 45 nm, a source/drain doping concentration of 10^{19} and 10^{20} cm^{-3} respectively for the seed and bulk layer, and a well implant concentration of approximately $1e^{18}$ cm^{-3}. In the poly etch process, a pattern dependence mask is generated real-time based upon a real time etch depth calculation. The pattern dependence mask is used to adjust the etch rate loading map at different locations and create a poly residue profile. Figure 2 displays the

computer-generated poly residue structure (left). The poly profiles at different elevations (fin top, middle and bottom) are shown on the right-hand side of Figure 2. These profiles are quite similar to the Si profiles seen in Figure 1, demonstrating that the simulation produces consistent results with those seen during actual silicon fabrication.

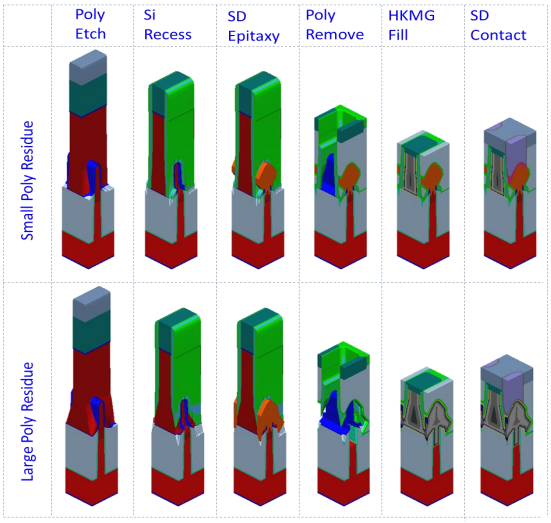

Figure 3: Defect evolution and failure mode analysis.

In the virtual fabrication platform, pattern dependent etch settings can be adjusted to produce poly residue structures of different sizes. Downstream processing can then be virtually performed based on the size of the poly residue structure, to better understand the defect evolution process and any expected failure modes. Figure 3 presents the expected feature evolution of a small poly residue structure and a large poly residue structure. The small poly residue downstream sequence does not create a hard failure mechanism within the structure. The larger poly residue sequence, however, can be exposed during the source/drain Si recess process and creates an abnormally large SD epitaxy. Due to the unexpected connection of enlarged epitaxy and poly residue, when the source/drain epi is replaced with metal gate material during the dummy poly remove and HKMG fill processes, finally poly to source drain epitaxy short is created.

To avoid this type of failure, a question needs be answered. How large of a poly corner etch residue is acceptable before a structural hard failure occurs? We investigated this question by modifying the poly residue width and height in virtual, experimental splits. We then observed if any source drain epi shorts were generated at the dummy gate poly during downstream processes, by checking the number of nets after the SD epitaxy process. As seen in Figure 4, the source, drain and gate can be separated into 3 different nets if the residue does not cause a short, while the number of nets will be less than 3 if the residue is too big and leads to an epi to poly short. Using this methodology, we tested 100 combinations of residue widths and heights in a virtual DOE to determine which combinations lead to an epi to poly short. Fig. 5 displays a contour map containing the number of nets compared to the residue widths and heights. The splits in the green area include proper (non-failing) device structures with 3 nets, while the yellow and orange areas denote splits with hard failures. Based upon these results, a residue width of about 8 nm is the limit before hard failures occur. However, when the residue height increases at this 8 nm residue width, the width margin becomes narrower (See Figure 5, red dotted line). Considering the potential manufacturing variability of both residue width and height (potentially 1.5 nm and 5 nm respectively), a "safe" residue window can be found on the left-hand side of the blue dotted line.

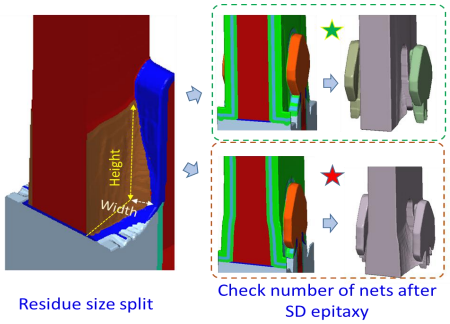

Figure 4. Poly residue width and height defect and number of nets under different residue conditions.

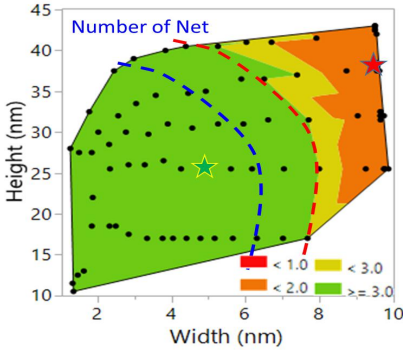

Figure 5: Contour map containing the number of nets compared to the residue width and height

IMPACT OF POLY CORNER RESIDUE ON DEVICE PERFORMANCE

Using an acceptable poly residue (with no hard failures), we then simulated device performance of a cropped 5 nm NMOS transistor using a built-in drift-diffusion solver in SEMulator3D. Figure 6 displays the I_D-V_G curve for different residue width and height splits (V_D=0.8 V). Larger residue width and height settings boosted device performance with higher on-current (108%) and lower off-state leakage (50%), compared with an ideal structure that had no residue. Figure 7 shows contour maps

of the major device performance parameters at different residue sizes. A larger residue produced benefit in on-state drive current, off-state leakage, subthreshold swing and DIBL. The only negative effect of a larger residue was an increase in parasitic capacitance between the source/drain and the gate. To further understand the mechanism of this device performance boost, we investigated the on-state and the off-state current distribution at the fin bottom when a larger residue was present (See Figure 8).

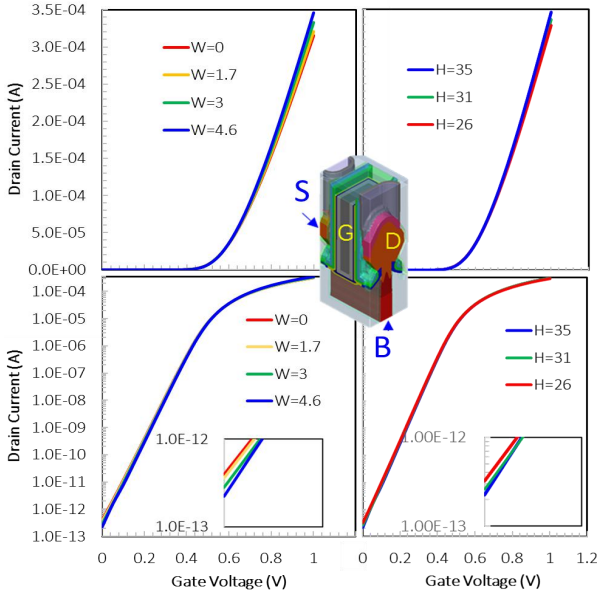

Figure 6: I_D-V_G curve of different residue size splits

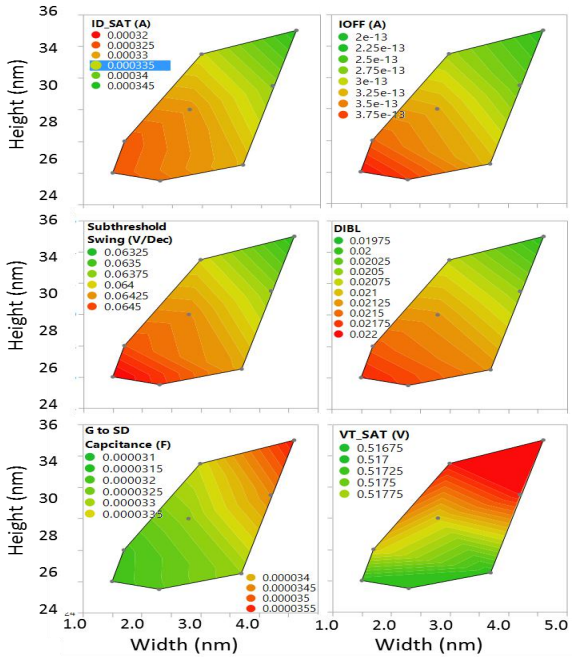

Figure 7: Contour maps of main device performance parameters as a function of residue size

During the on-state, the channel length becomes larger when the poly residue is present. The residue covers part of the access area between the source/drain and the gate. Series resistance consequently is smaller, leading to a larger drive current. During the off-state, most of the fin area between the source and the drain can be controlled by the gate. Consequently, the resistance between the source and drain is higher when a poly residue is present and provides lower off-state leakage.

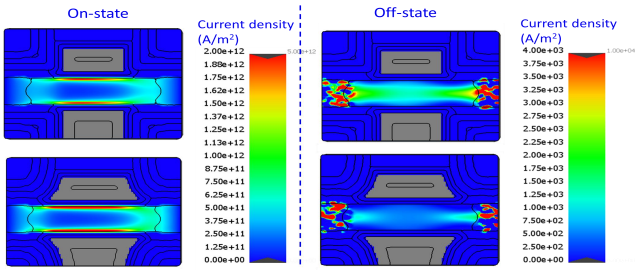

Figure 8: On/off-state current distribution at fin bottom (top figures: no residue; bottom figure: with residue).

CONCLUSION

In this paper, poly corner residue during a 5 nm FinFET poly etch process was modeled in the SEMulator3D virtual fabrication platform using a pattern dependent etch function. A virtual DOE was completed to gain a greater understanding of acceptable process windows and associated device performance at different poly residue dimensions. The results establish that an excess poly residue width and height leads to a hard failure (short) between the source/drain epitaxy to metal gate. A properly-sized poly corner residue can boost device performance compared to having no residue, with a greater than 8% on-state current increase and approximately a 50% off-state current drop. This occurs due to the reduction of access resistance between the source/drain and gate during the on-state, and better gate control in the off-state. Our study demonstrates that instead of completely minimizing poly corner residue, poly residue size control can be implemented to gain device performance and concurrently maximize yield.

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