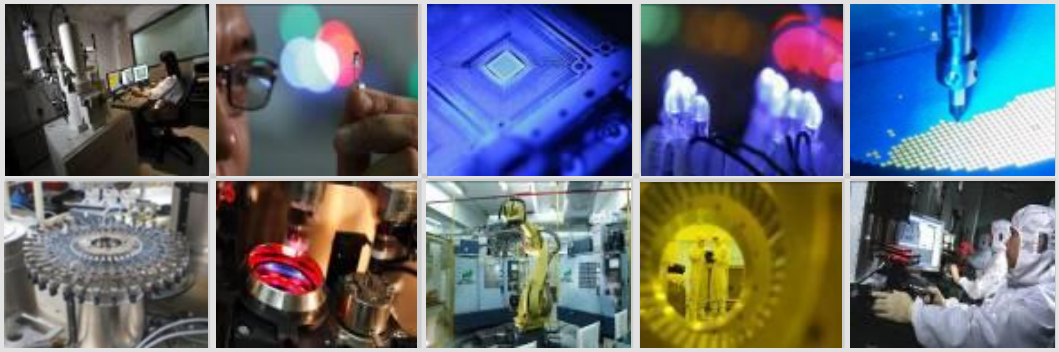
Advanced Packaging Technologies Update



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Presentation outline

- Advance Packaging Technologies driving forces
- New trend in WLCSP (Mold Protected WLCSP)
- Advance FC interconnect Technologies
- Various FanOut Technologies
- FanOut Process and material consideration

Advance Packaging Technologies Driving Forces

PC/Notebook

- Cost
- Hi Performance

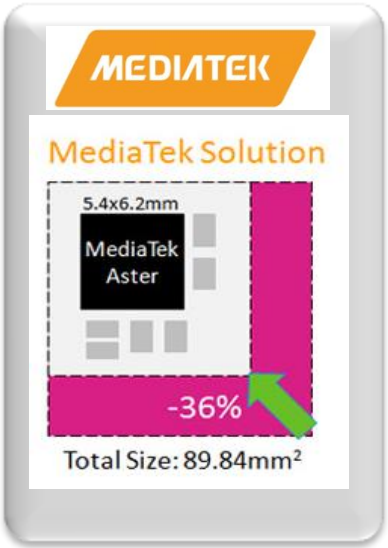
Mobile/Tablet

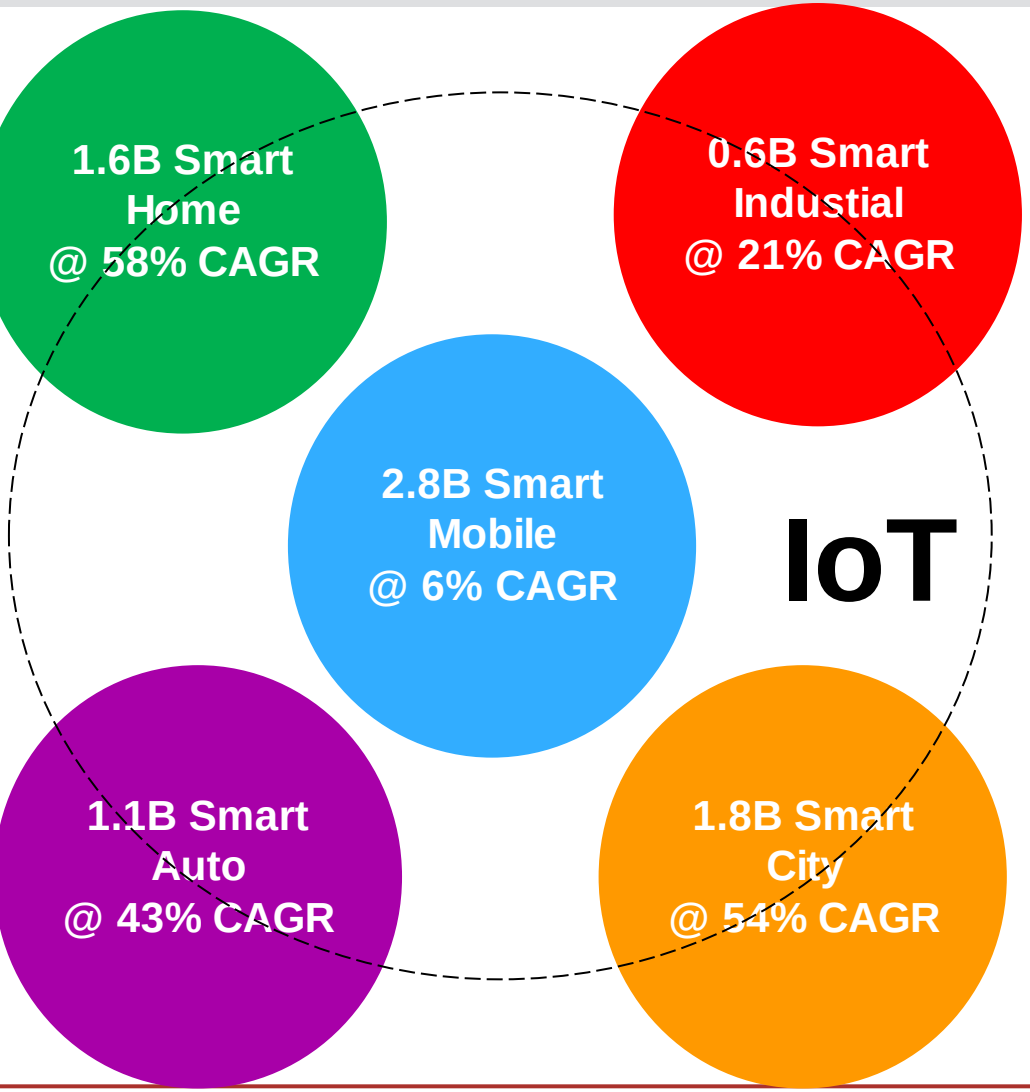
- Low cost but hi vol.
- High Performance
- Miniaturization
- Low power consumption

- Lower cost but higher vol.
- Mid & High Performance
- High speed connection
- Miniaturization
- Low power consumption
- Fab-like technology
- Embedding technology
- Fusion/combo structure

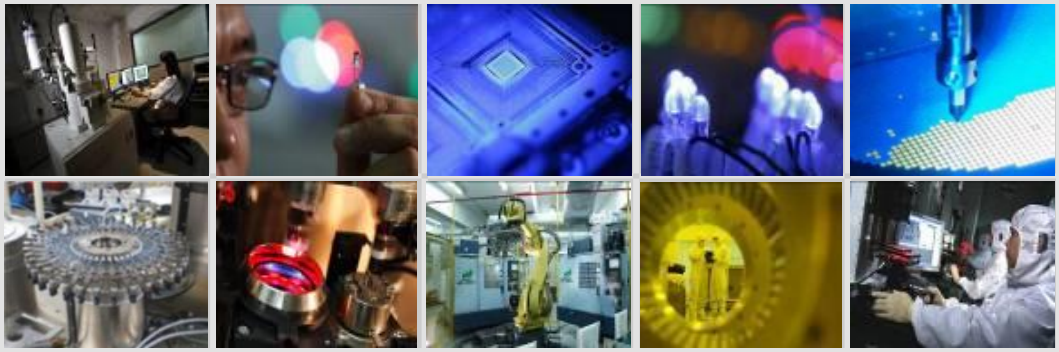
Integration	SoC	SoC / SiP	Advanced SiP
Products	CPU / GPU / Wireless / Memory	AP / PMIC / RF / Wireless / Memory / Touch IC / CIS	AP/ Micro processor / PMIC / RF / Wireless / Memory / CIS, MEMS & Sensors
Format	Singulated, Low density strip	Strip Block Matrix	Hi density strip block matrix, Wafer, and Panel form

Explosive growth expected for IoT by 2020
Expected number if IoT device to be shipped in 2020





New trend in WLCSP for both IC & Discrete



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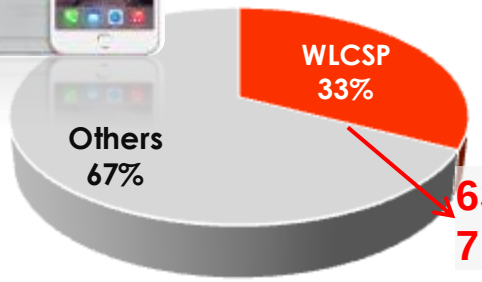
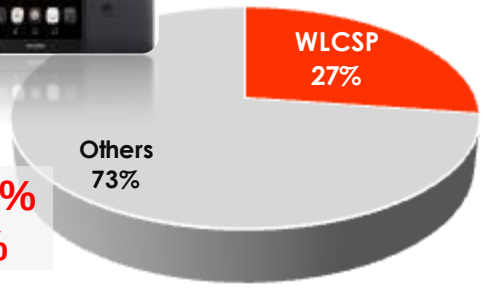
Wafer Level Packages

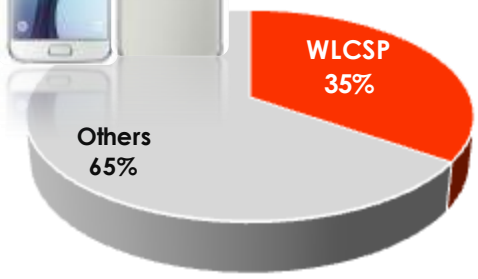
iPhone 6+



Huawei Ascend Mate 7

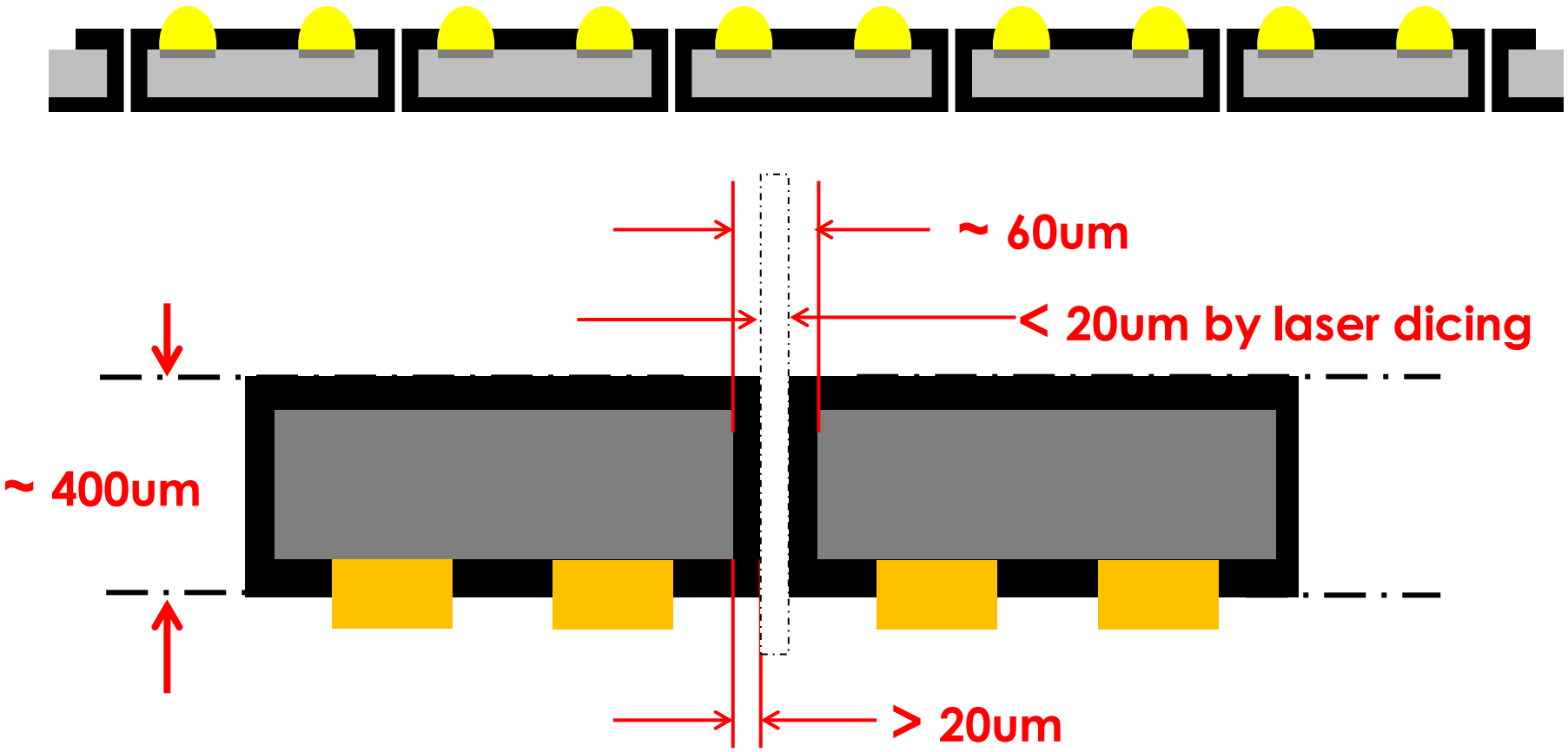


Samsung Galaxy S6

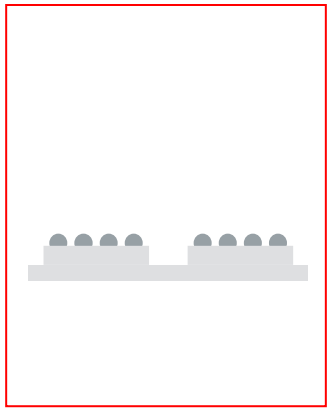


6S : 40%
7 : 41%

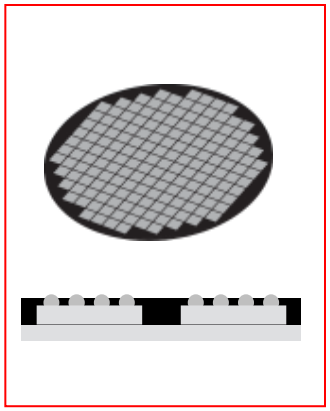
Mold Protected WLCSP



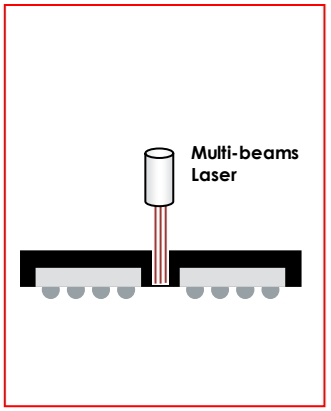
Mold Protected (mpWLCSP) Solution



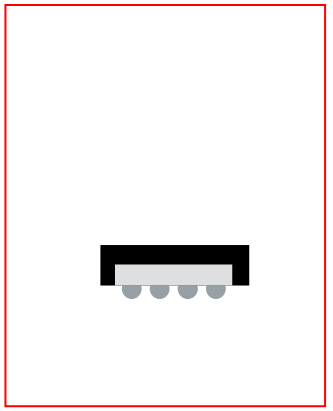
1 Ball Drop



2 Molding



3 Laser Singulation



4 WLP Inspection, Test & Packing

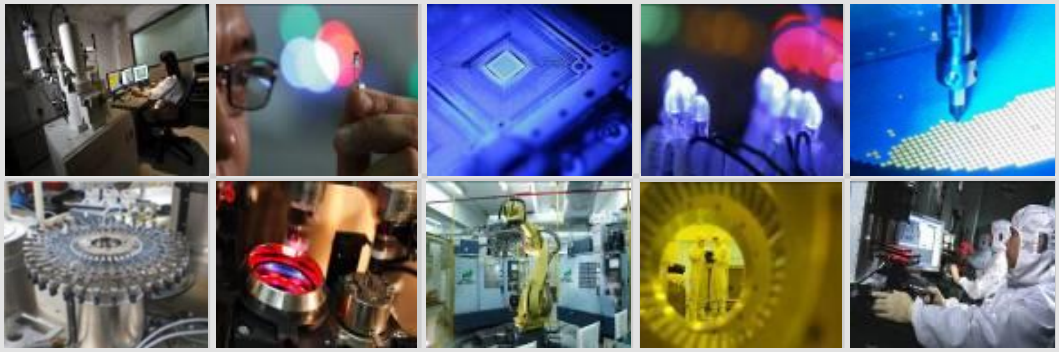
DEK GALAXY

ORCAS

LASER1205

SUNBIRD

Advance Interconnect Technologies



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Advance FC Interconnect Model

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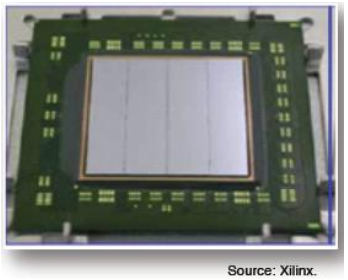
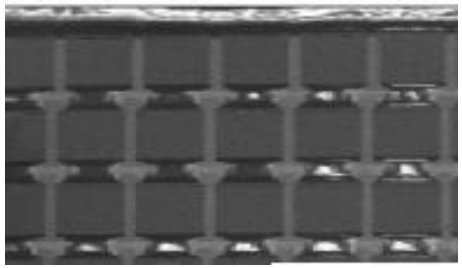
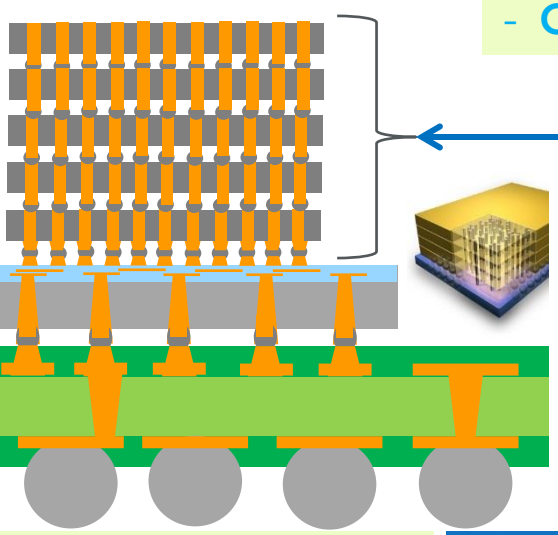
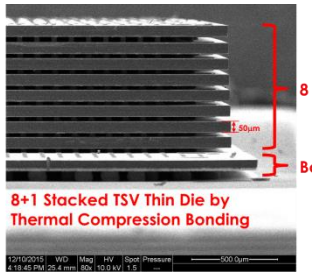
- ~ 40 um pitch, micro pillar bump
- 2.5D Si/Glass Interposer
- for multi-die (Die partition & Hetero-integration)
- MR & TCB (Fluxless TC LPC, TCCUF, TCNCP)
- C2S, C2W





- 10 to 40um pitch
- U pillar bump
- 3D TSV Dies Stacking w/ TC Bonding (FluxLess TC LPC, TC NCF)
- C2C2S, C2C2W





- 50um to 130um pitch
- C2 (Cu Pillar) & C4 bump tech.
- MR & TCB (TC LPC, TCCUF & TCNCP)
- HD BuildUp substrate, Multilayers laminate, MIS, & L/F
- C2S, C2P

ASM Advanced Packaging Total Solution

Key Features	AD8312FC	AD9212+	Firebird S	Firebird W	Nucleus	Nucleus XL
Accuracy @3σ	±10um	±5um	±2um	±2um	±2.5um (Local FC)	+/-5um (Global FC)
Alignment Mode	Local	Local	Local	Local	Local & Global	Local & Global
Placement Mode	DA & FC	FC	FC	FC	DA & FC	DA & FC
Max. Bond Force	30N	15N	30N	30N	300N	30N
Bond Collet Heating	-	-	Pulse, 400°C max	Pulse, 400°C max	Const,350°C max	Const, 200C max, Optional
Stage Heating	-	-	200°C max	200°C max	250°C max	-
Max. strip size	100x300 mm	210x323 mm	125x250 mm	300 mm ø	300 mm ø, 340x340 mm	670x600 mm
C2W	-	8”	-	Upto 12”	Upto 12”	-
Die Size	0.25 – 10mm^2	0.5 – 30mm^2	2x2 – 33x22mm^2	2x2 – 33x22mm^2	0.5 – 25mm^2	0.5 – 25mm^2
Die Thickness	50um	50um	50um	50um	50um	50um
Fluxer	✓	✓	Opt	Opt	Opt.	Opt.
Dispenser	Opt. (Dual)	-	-	-	-	-
Multichip	-	-	✓ TnR	✓ TnR	✓ Multi-die ejector	✓ Multi-die ejector
Class100	-	-	✓	✓	✓	✓
Tape & Reel	-	-	✓	✓	-	-
Application	FCOL	C2W, FCCSP, FCBGA	C2S TCCUF, 2.5D & 3D	C2W TCCUF, TCNCF 2.5D & 3D	2.5D, FOWLP/PLP, Active Embedded	2.5D, PLP, Active Embedded

Advanced Interconnect Solution

ASM

C2/4 FC + MR

8" C2W

12" C2W

WLFO 330x330

PLFO 600x600

TCCUF TCB TCNCF

AD8312FC Plus

UPH: 12K
Acc: 15µm
FC SOT
FC LGA
FC QFN

AD9212Plus

UPH: 6K
Acc: 5µm
FC CSP
FC BGA
FC C2W 8"

Next Gen under Development
UPH: 8K
Acc: 3µm

Nucleus

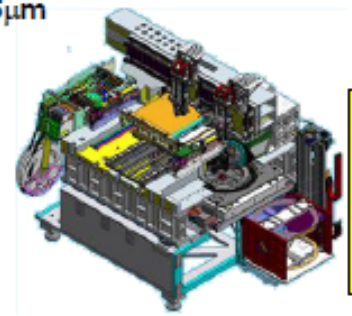
DD-L: 5K, 2.5µm
DD-G: 6K, 3.5µm
DU-L: 4K, 4µm
DU-G: 5K, 5µm
2 BH, 2 BS
TC BH UPH:
DD-L: 3.6K
DD-G: 4K
DU-L: 3K
DU-G: 4K

Nucleus XL

DD-G: 5K, 3.5µm
2 BH, 1 BS

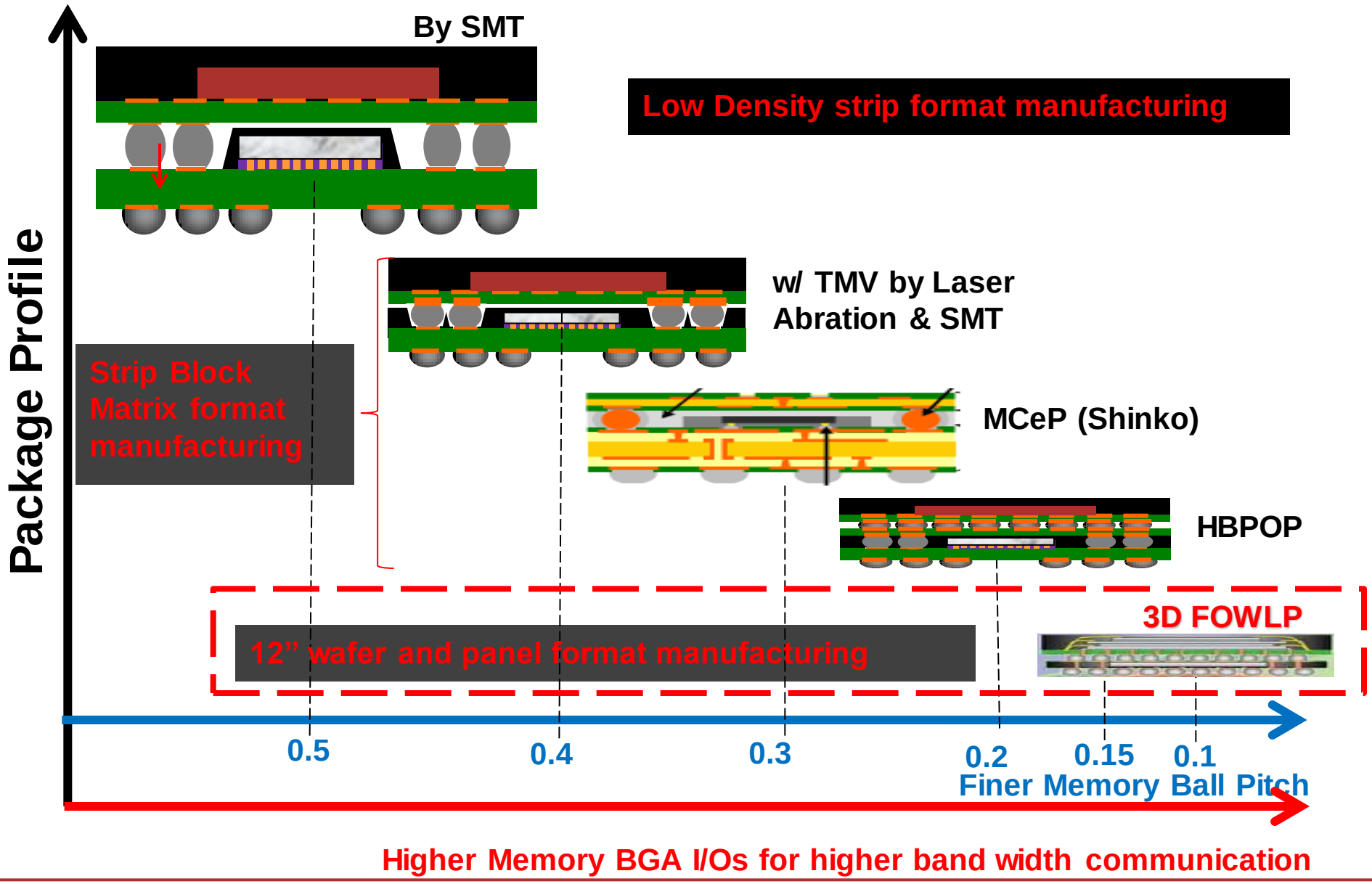
Firebird C2S/C2W

Acc: 2µm
1 BH, 2 BS (C2S)
1 BH, 1 BS (C2W)
Inert environment
Nozzle change (MCM)



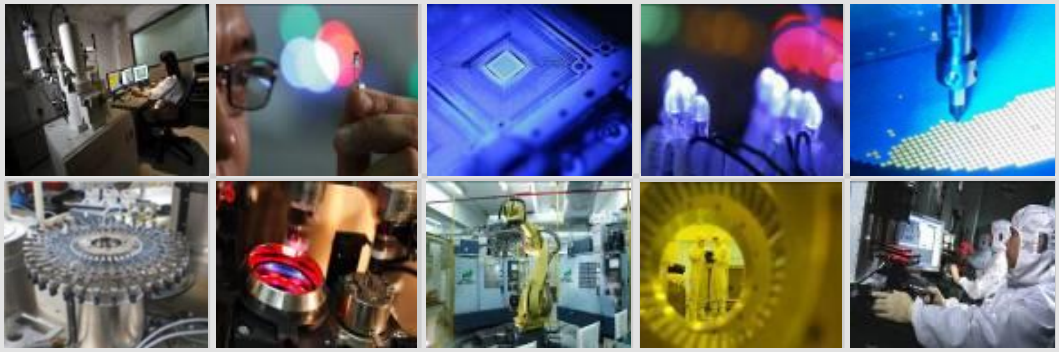
Neuron SiP under Development
UPH: 7K
Acc: 5µm

AP POP Evolution Trend



Various FanOut Technologies as the alternatives

ASLAC: Accuracy, Speed & Large Area Capability



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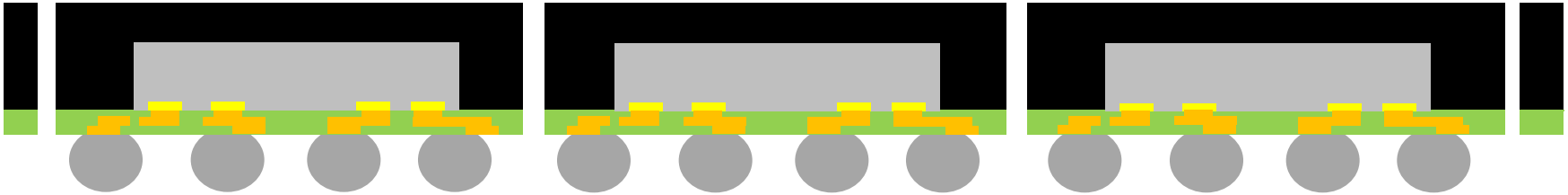
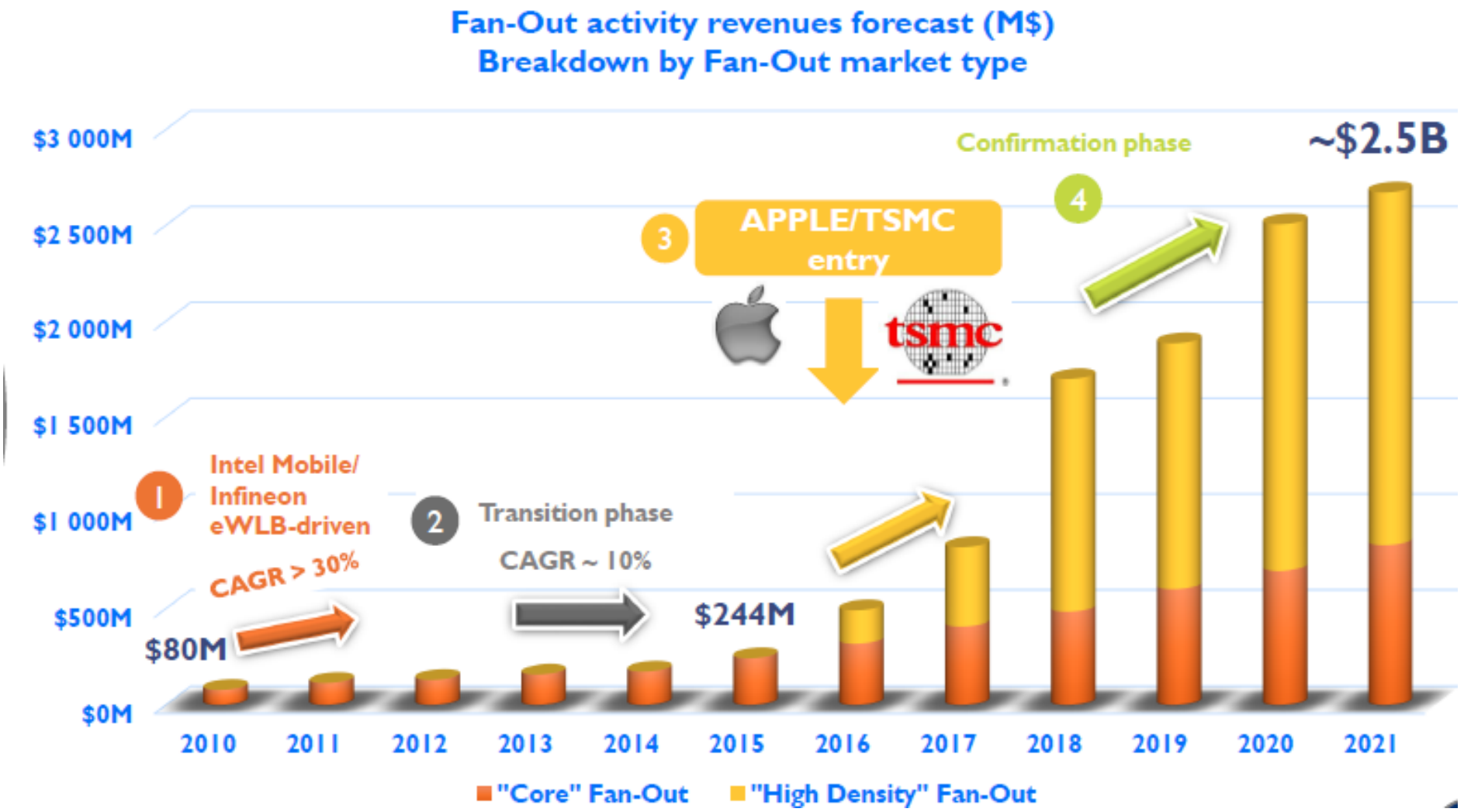
eWLB (embedded Wafer Level BGA by Infineon)



Process:

- 12” wafer format
- Low density RDL
- Die 1st, Die Down, Global Alignment

Yole's FOWLP Forecast

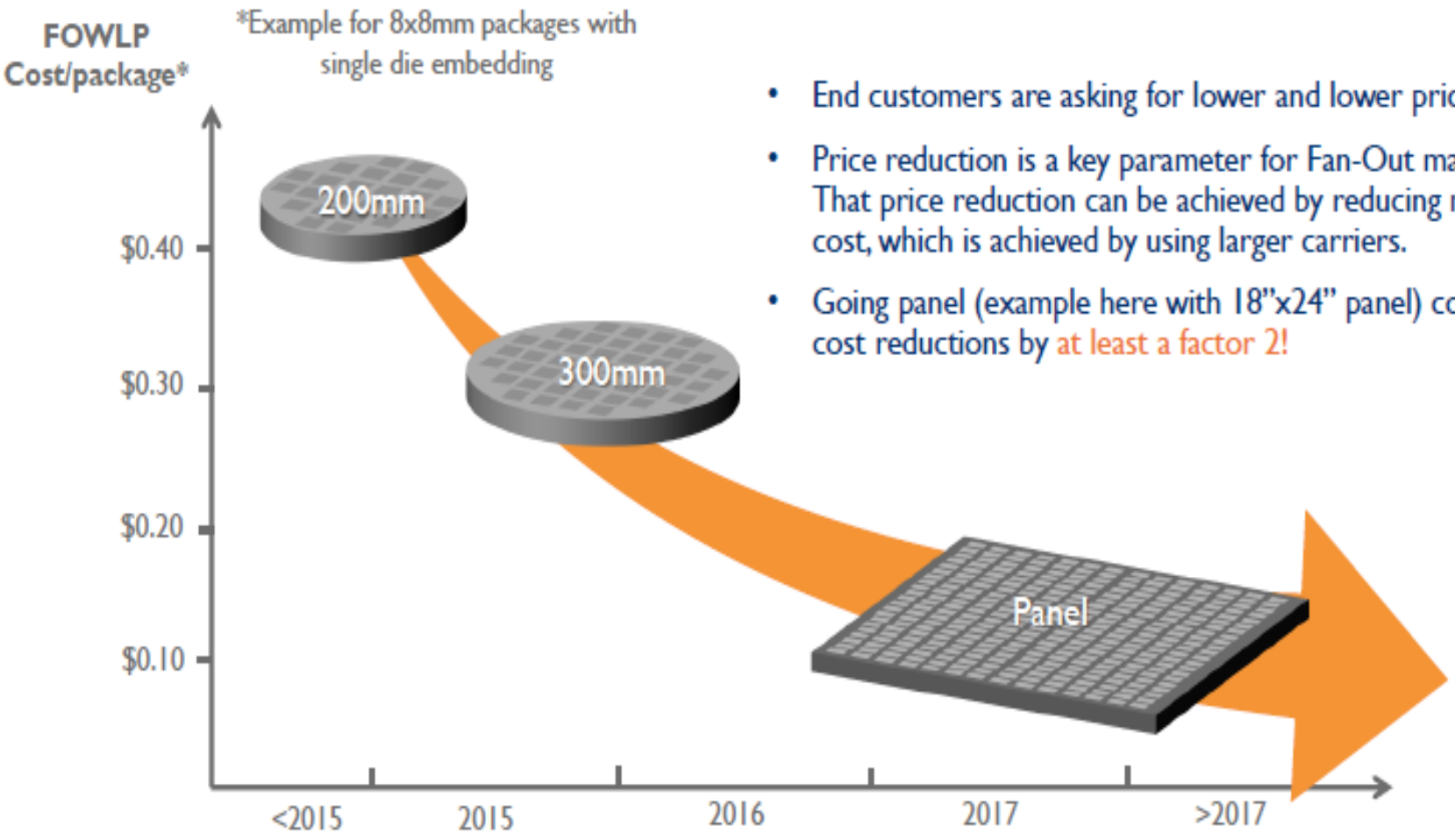


Taking off of Fan Out Technologies

The Power of Fanout Technologies

Today	Starting & under development	Features and applications
2.5D with TSV Interposer **CoCoS/ CoWoS** **w/ TCB, MR**		
HBPOP **(with Substrate Interposer)** **w/ TCBNCP, MR+MUF**		
FCCSP (ETS, MIS) **w/ MR+MUF**		

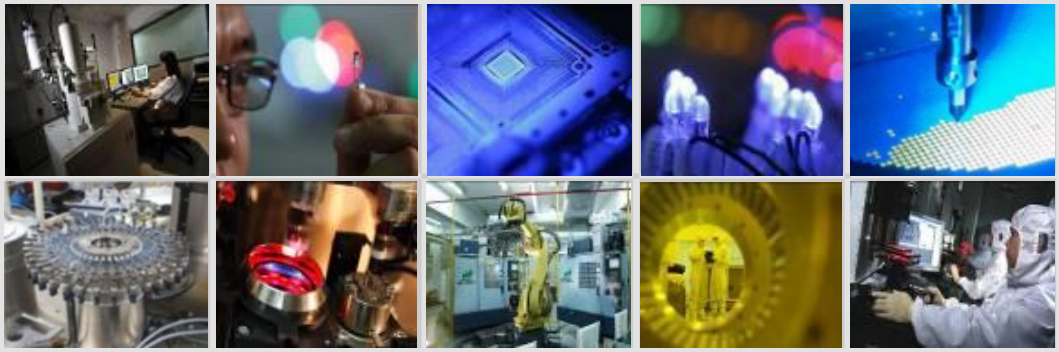
Fanout cost evolution



- End customers are asking for lower and lower prices.
- Price reduction is a key parameter for Fan-Out market growth. That price reduction can be achieved by reducing manufacturing cost, which is achieved by using larger carriers.
- Going panel (example here with 18"x24" panel) could enable cost reductions by at least a factor 2!

Process and Material consideration for Fanout Technologies

ASLAC: Accuracy, Speed & Large Area Capability



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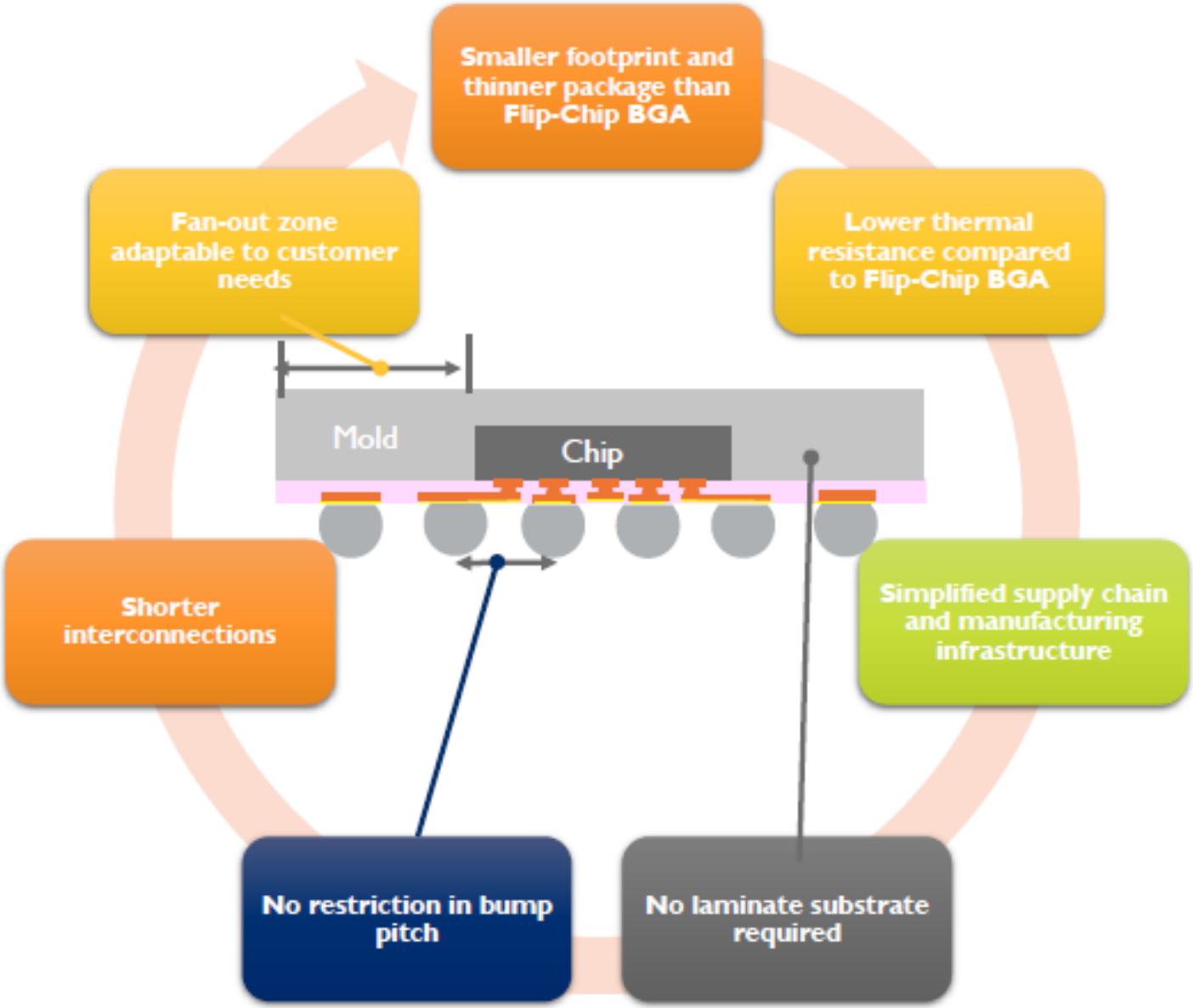
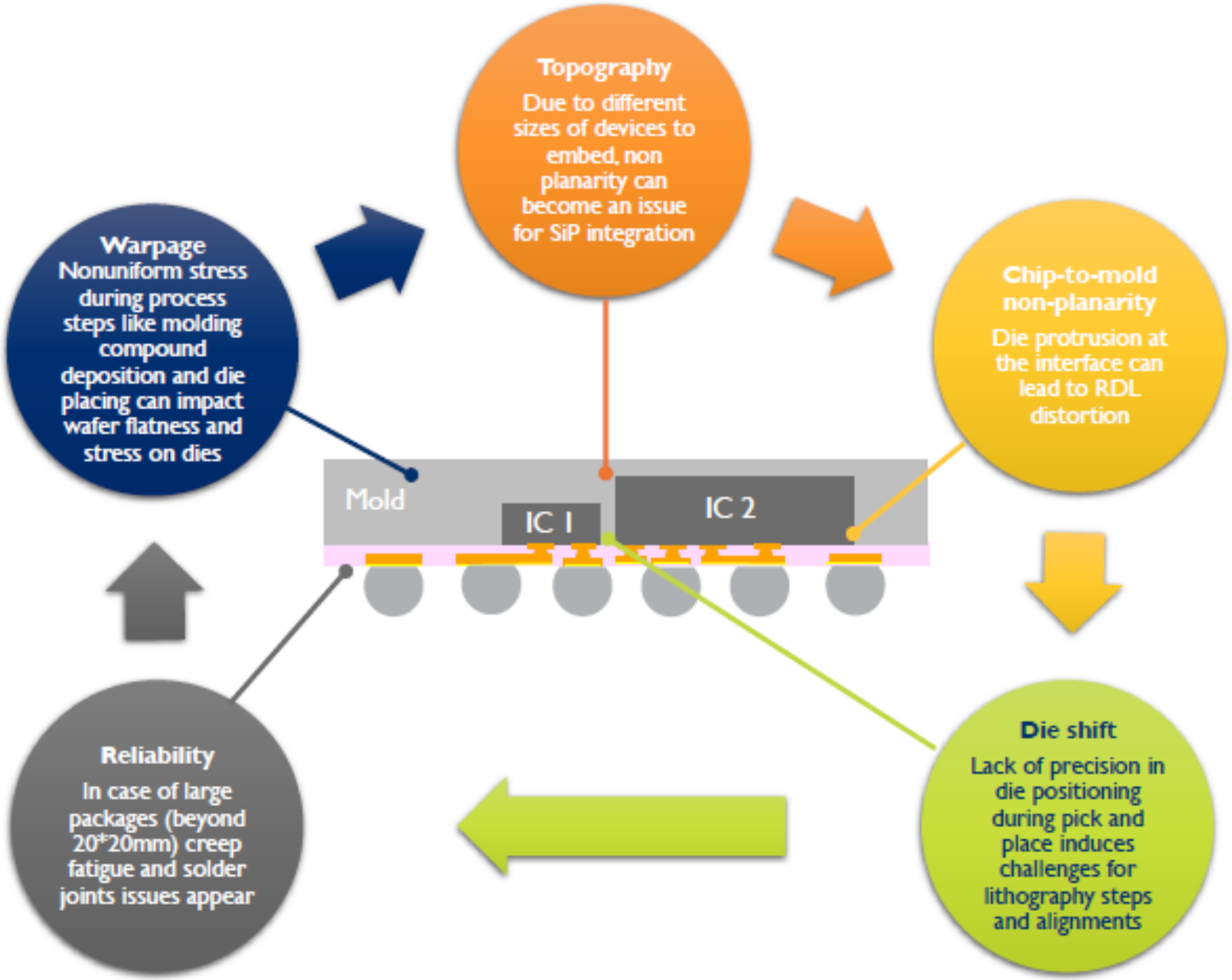
eWLB Advantages



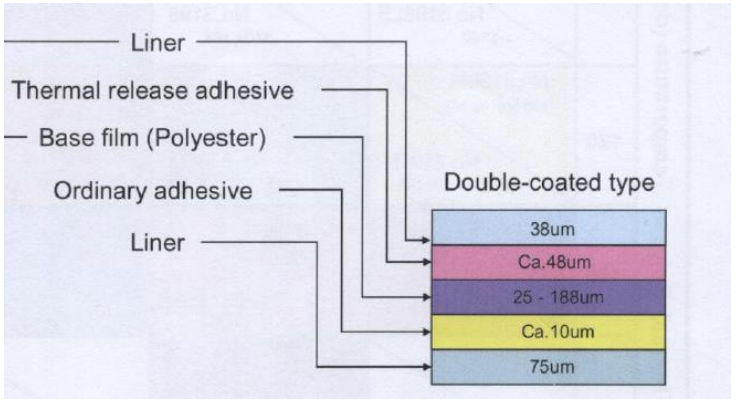
- Better 2nd level reliability than WLCSP
- Excellent electrical performance
- RoHS & REACH compliant
- Low profile, miniaturized high performance package
- No substrate, no bump, no flux no reflow, no underfill

Technical Challenges

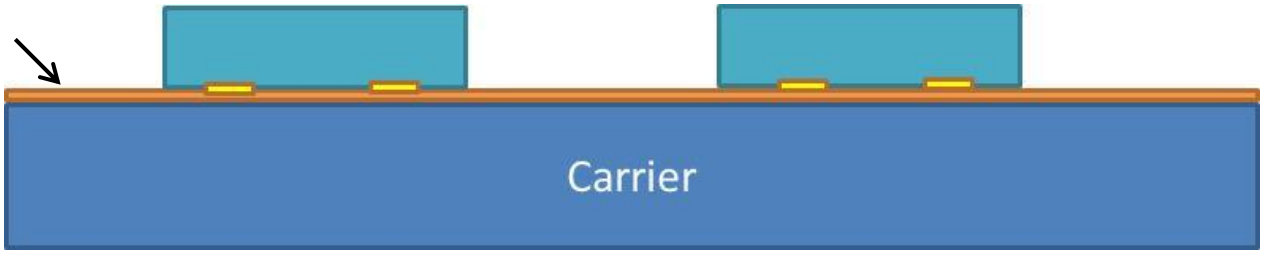


Adhesive Film for Die Down Attach

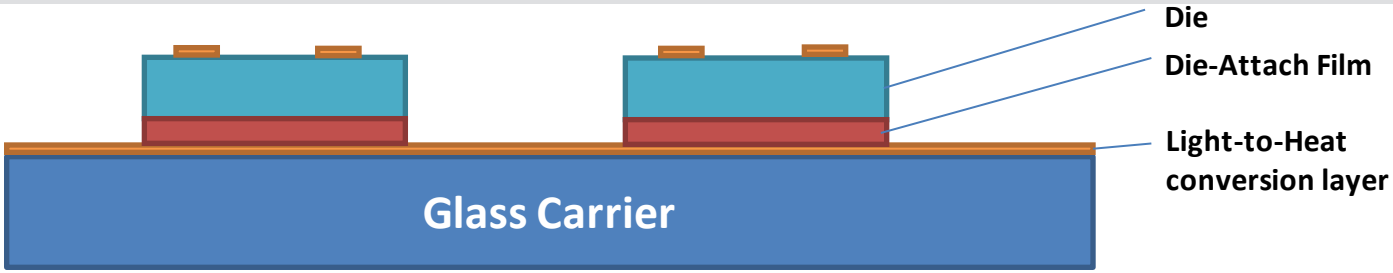
- **Thermal release tape**
  - **Chip first (Die down) structure**
  - **Temporary bonding**
  - **Good adhesion during molding**
  - **Easy release at a higher temperature**
  - **Thickness: 100 - 150 um**
  - **Lamination on the carrier**



Revalpha from Nitto Denko



Adhesive Films for Die up Attach



- **DAF and LHTC**

– Chip first (Die up) structure

– Die Attach Film (DAF) Thickness: 15 – 25 um

– A Light to Heat Conversion Layer (LTHC): a sacrificial layer for debonding

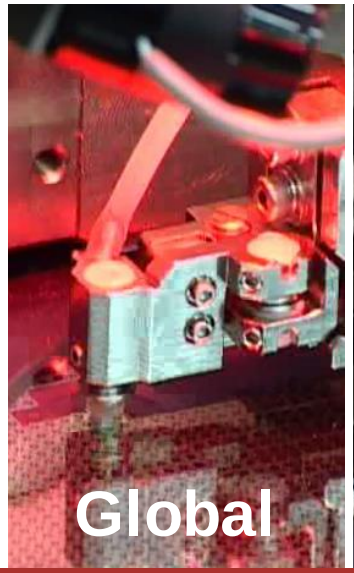
– Compatible with typical semiconductor chemistries and processes

– Excellent adhesion

– Low modulus, High Tg, thermal stable at subsequent RDL process

DAF	Tg	Elastic Modulus (150C)	Bonding temperature	Bonding Pressure
Hitachi	180C	6 MPa	100 -160C	0.05 -0.2 Mpa

Pick and Place Die Attach Process



Many different process approaches with the same manufacturing format

- **Chip 1st / RDL 1st (Global / Local alignment)**
- **Die down / Die up**
- **Flux dipping for high accuracy C2W FC process**
- **High bond force with elevated bond temperature for DAF bonding**
- **Compensation for die shift**

Accuracy Performance

NUCLEUS Placement Accuracy to Support Different Process Need

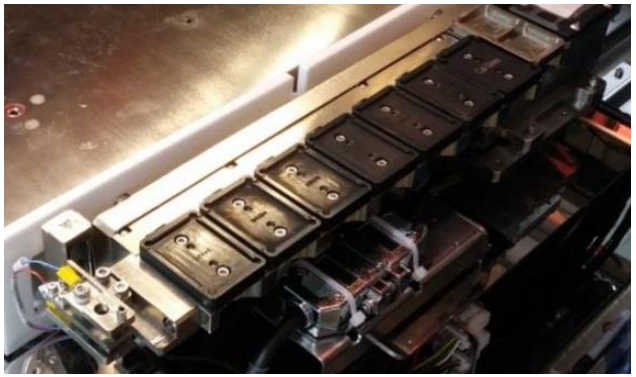
Flip Chip (Die Down Mode)	Local Alignment	+/- 2.5um
	Global Alignment	+/- 3.5um
Die Bond (Die Up Mode)	Local Alignment	+/- 4um
	Global Alignment	+/- 5um

MCM Process Capability

Automatic Collet and Ejector Tool Change

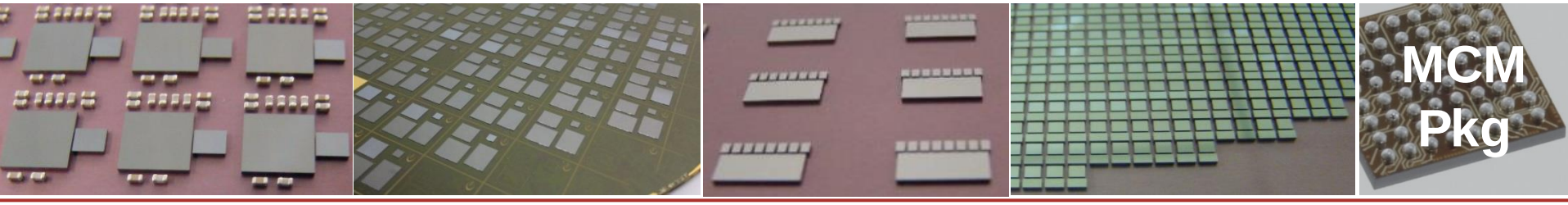
Automatic Bond Collet Tool Change

- Automatically change bond collet tools for different die size in MCM pkg
- Support 4 – 5x different die size collet tool change



Multiple Die Ejector System

- Automatic changer for die ejector
- Support up to 5 different types of ejector kit installation
- Synchronize needle motion with bond head and flipper
- Support die size up to 30mm

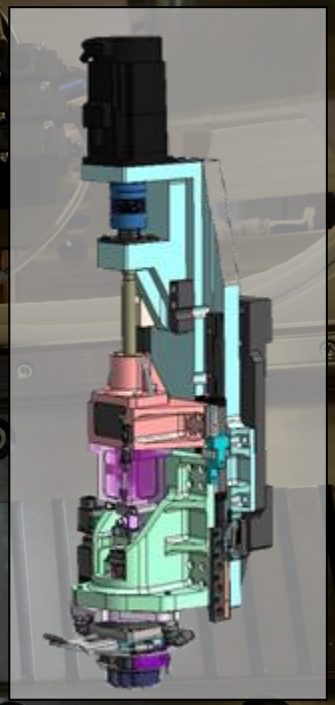


Flexible Process capability

Thermal Compression Bond Head and Light Bond Head

Thermal Compression Bond Head (Ready)

- Bond force: 10 – 300N
- Bond force accuracy:
  - < 40N: ±2N
  - > 40N: ± 5%
- Collet Heating: 350˚C
- Heating mode: Continuous
- Bond head rotation of ±15˚ for fine bond accuracy adjustment



Light Bond Head (To be available in Q3)

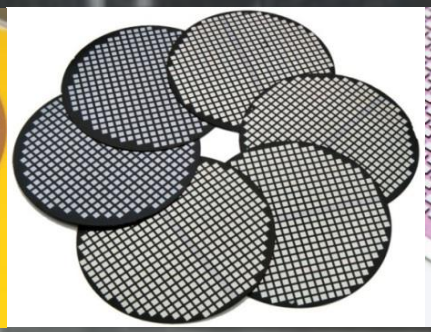
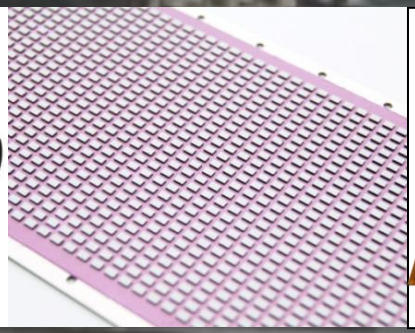
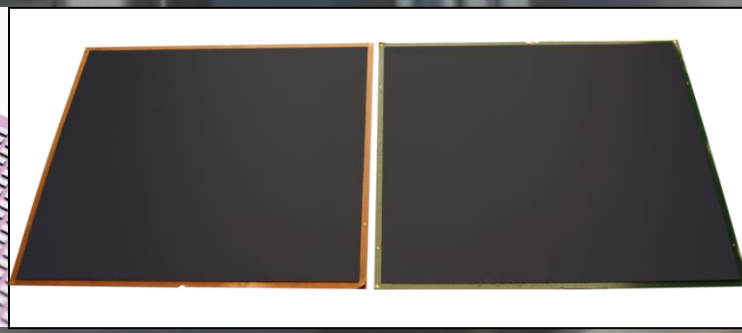
- Bond force: 0.5 – 10N
- Bond force accuracy:
  - < 2N: ±0.1N
  - > 2N: ± 5%
- Bond head rotation of ±15˚ for fine accuracy adjustment

Suitable for Different Format

Large Format Handling – Round and Quad

Large Work Holder Design

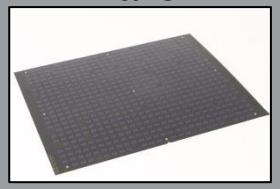
- To support up to
  - 12” Wafer Substrate / Carrier
  - 330 x 330mm² Panel Substrate / Carrier
- 12” wafer with auto load/unload
- Support Work Stage heating up to 250˚C
- Integrated equipment solution for FOWLP, FOPLP and Active Embedding

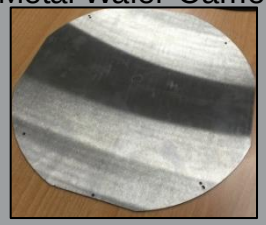
Multiple Material Handling System Configurations

Compatible with Different Material Format

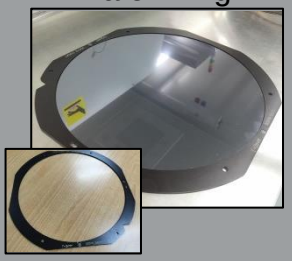
Panel



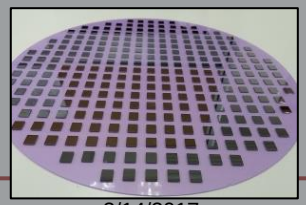
Metal Wafer Carrier



Wafer Ring



Wafer / Glass Carrier

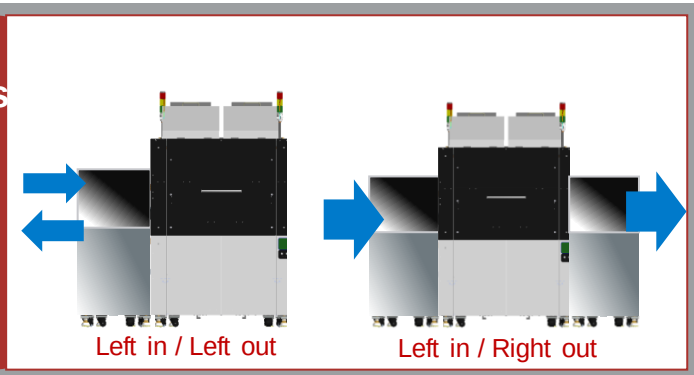


Cassette

FOUP

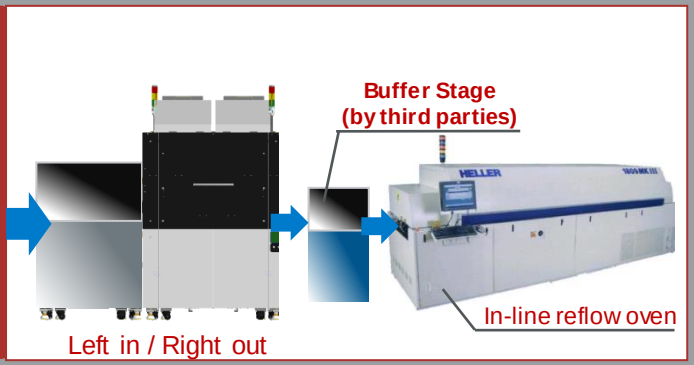
STANDALONE with CASSETTE LOADER/s

- Cassette in / Cassette out
- Left in / Left out or
  Left in / Right out
- Wafer on ring / Panel



INLINE with CASSETTE LOADER

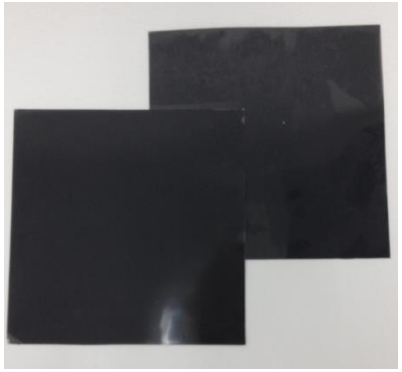
- Cassette in
- Inline with reflow oven
- Left in / Right out
- Wafer on ring / Panel



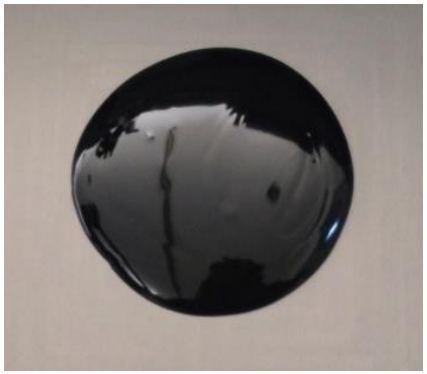
EFEM / NUCLEUS COMBO

- With EFEM System
- FOUL cassette handling
- 8”/12” wafer substrate

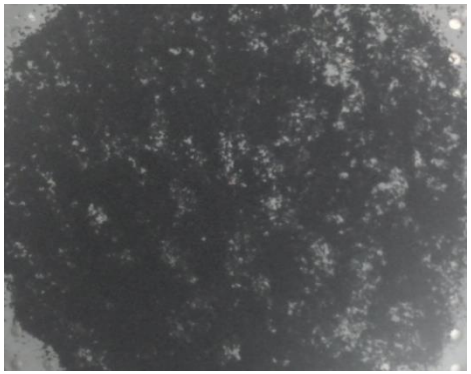
EMC Materials for FOWLP



Sheet/B-stage



Liquid (automation)



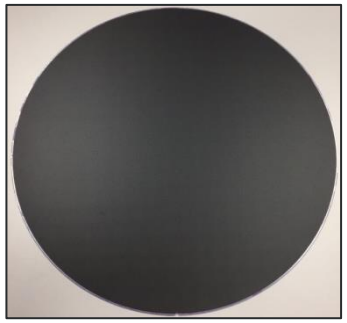
Granular (automation)

	Thinner Package	Product performance	Productivity	Cost-effective	Scalability
Sheet	+++++	+++++	+++	++	+++++
Liquid	++++	++++	+++	+++	++++
Granular	+++	++++	+++	+++++	+++

	Filler content (%)	Filler size (average/maxum)	CTE (ppm/C)	Young's modulus (GPa)	IMC (OC/min)	PMC (oC/min)
Nagase (R4507)	85	8/25	10	19	125/10	150/60
Sumitomo (G730)	90	55	7	30	125/10	150/60

Technical Challenges for Compression Molding

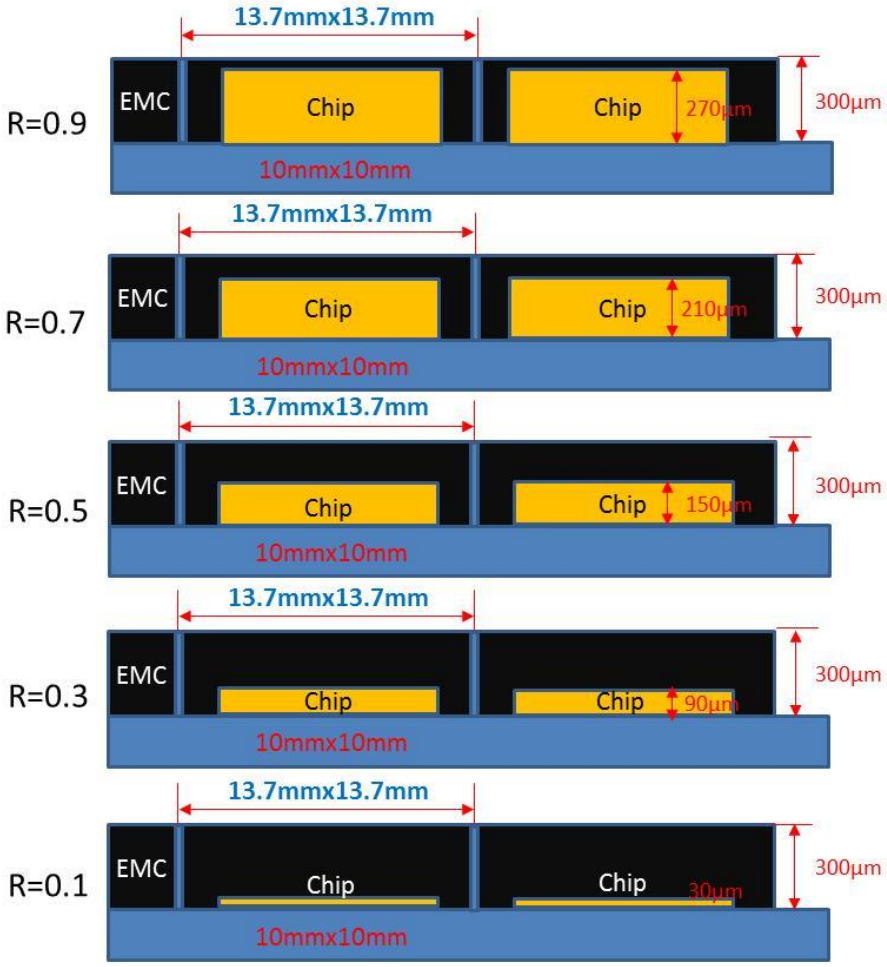
- **Die Shift**
  - Molding Process optimization
- **Dispensing**
  - In particular thin mold cap of less than 100 μm
- **Moldability**
  - Co-planarity – TTV of 20 μm get more challenging with increase size
  - Flow mark due to dispensing limitation for thin mold cap and material formulation
  - Incomplete fill due to poor process optimization and low vacuum level
  - Mold Bleed on die due to de-bonding of thermal tape
  - Film wrinkle is translated on the molded panel or wafer due to larger size, as maintaining tautness of film during compression is challenging
- **Warpage Control**
  - EMC with low CTE and low modulus
  - CTE Matching between EMC, adhesive films and carrier materials



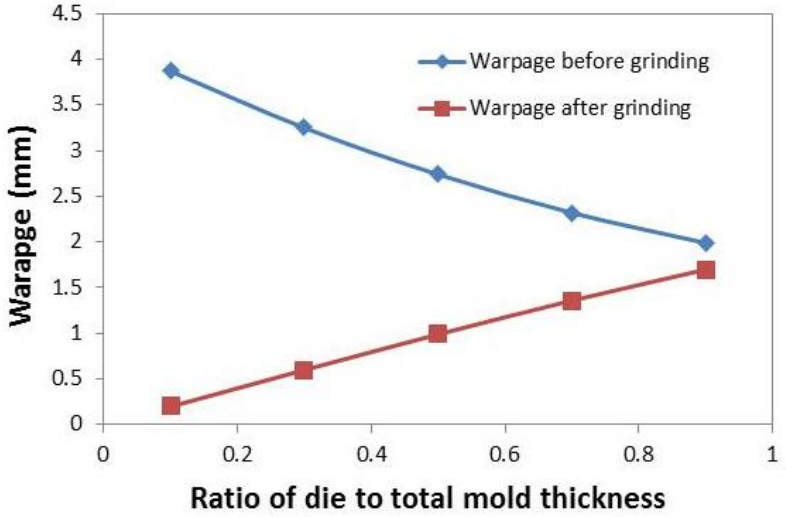
Warpage being the Major Challenge

- **Package Design**
  - Volume ratio of die to EMC
  - Die/Package thickness
  - Die to package fan-out ratio
- **Material Selection**
  - EMC
    - CTE, Modulus
  - Temporary carrier
    - CTE, Young's modulus
  - Adhesive
    - Young's modulus, thickness
- **Process optimization**
  - Bond force
  - Temperature

Effect of Die Thickness on Warpage



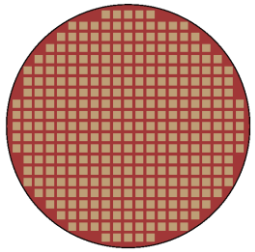
- ***The warpage before grinding decreases as increasing the die-to-mold thickness ratio***
- ***↑ Die thickness ratio → ↑Si percentage in molded wafer → ↓CTE for molded wafer → ↓ warpage***

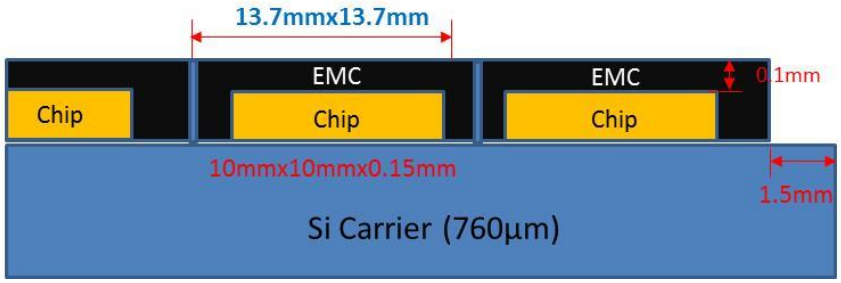


- ***The warpage after grinding increases as increasing the die-to-mold thickness ratio***
- ***↑ Die thickness ratio → ↓Si percentage in grinded wafer → ↑CTE for molded wafer → ↑Warpage***

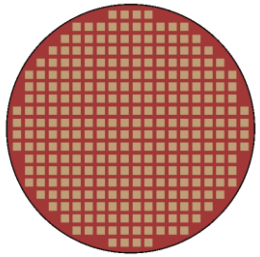
Effect of Fan-out Area Ratio on Warpage

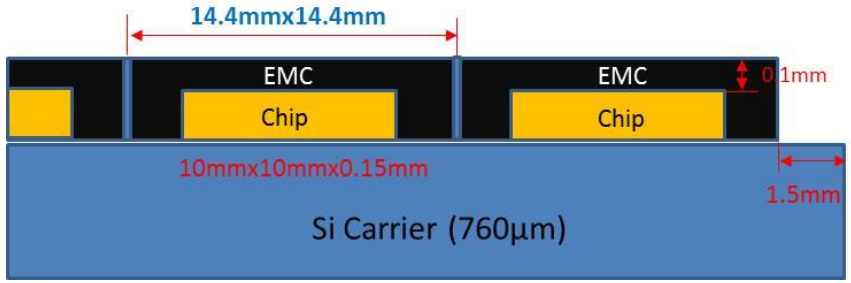
Package/die area ratio: 1.8
Die quantity: 341
12 inch carrier

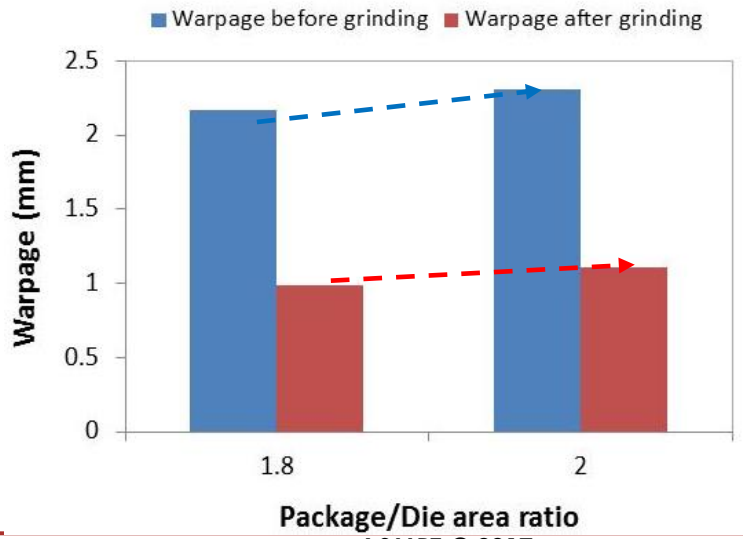




Package/die area ratio: 2.0
Die quantity: 300
12 inch carrier







- ***↑Fan-out ratio → ↓Si percentage in molded wafer → ↑CTE of the molded wafer → ↑ warpage***
- ***Warpage in both stages increases with increasing the fan-out ratio***

“ASLAC” for WLP & PLP (2.5D & 3D)

ASM

ASLAC = Accuracy

(2.5 um to 10um)

+

Speed

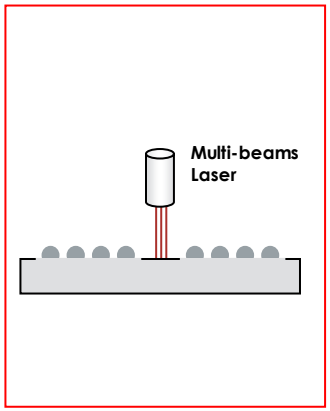
(5k to 25k uph)

+

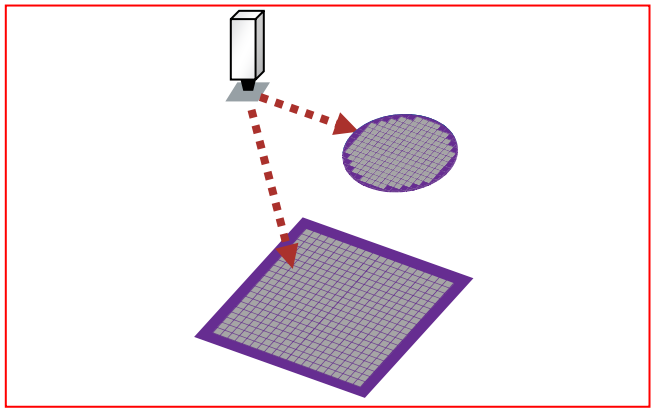
Large Area Capability

(300 Ø to 600x600 mm)

“ASLAC” for WLP & PLP (2.5D & 3D)

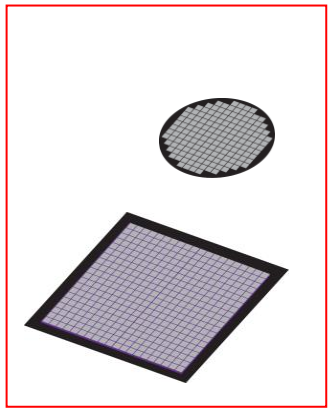


1 Thin wafer dicing

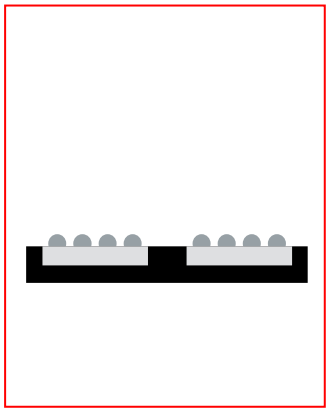


Pick n Place

2 TC Bonding



3 Molding



4 Ball Drop

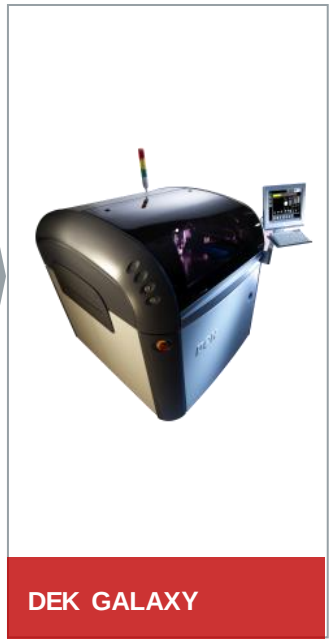
LASER1205

Precision WLP & PLP
NUCLEUS

WLP & Large PLP
SIPLACE CA

Firebird W

ORCAS



DEK GALAXY

ASM

Together We Can

ASM Pacific Technology
Innovation and Technology Leader