SEMICON® CHINA

Innovative 3D-SiP Package Technologies for More than Moore Era

Presented by

Albert Lan

藍章益

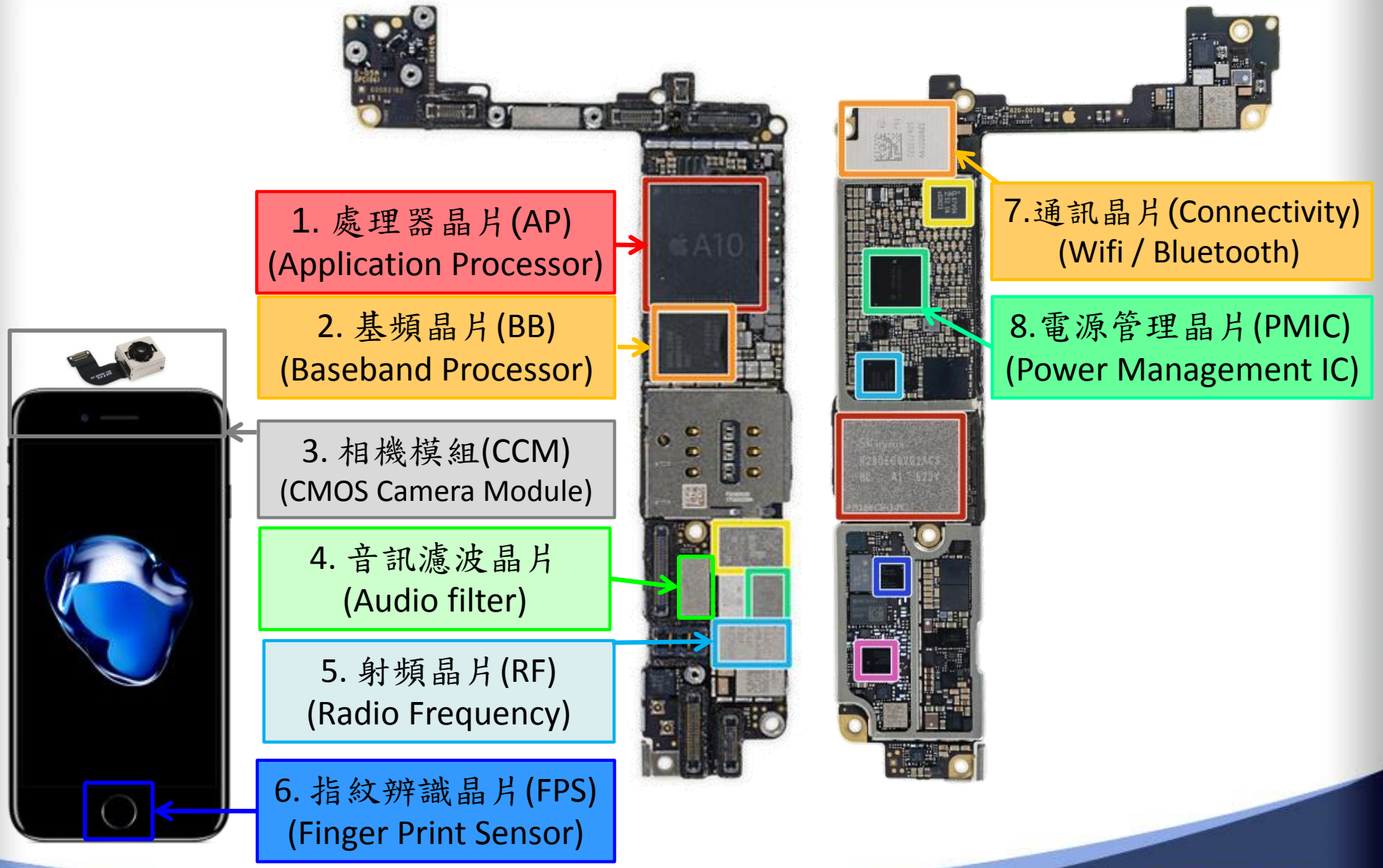
SPIL

15/Mar-2017

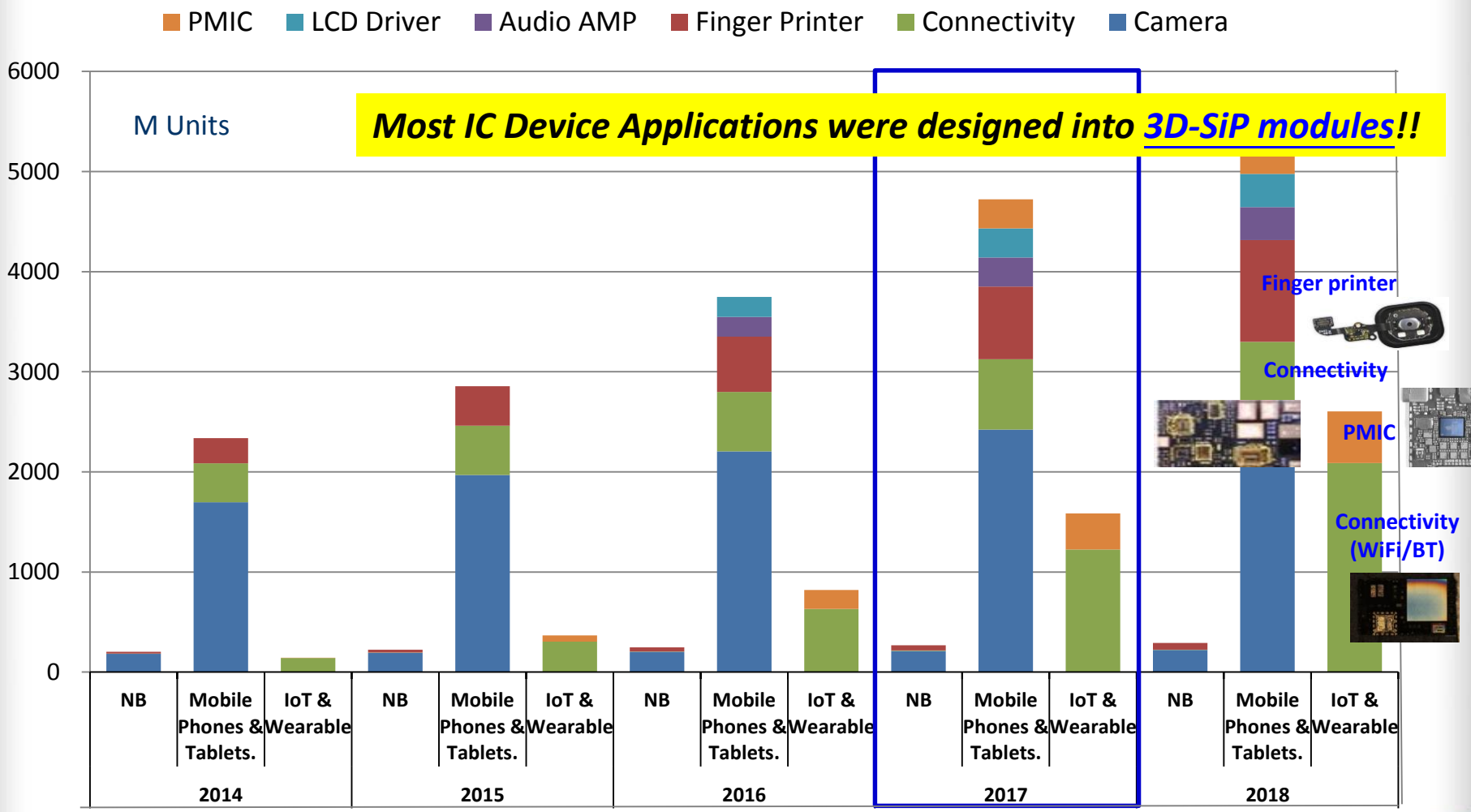
Outline

- ***Packaging Trend of SMART Phone/ Wearable/ Networking Devices***
- ***Innovative 3D-SiP Packaging Technologies***
- ***Summary***

IC Device Applications in Mobile



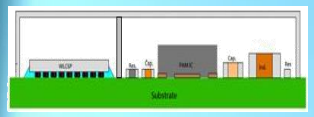
3D-SiP Market Growth Rate Overview



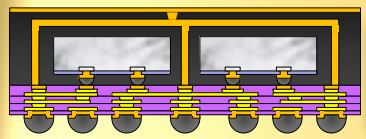
Source: Gartner, Morgan Stanley, Market Information

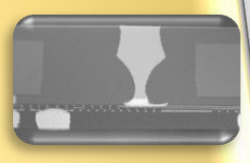
Innovative 3D-SiP Package Technologies

I. SiP TECHs

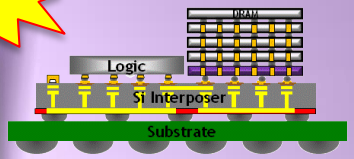


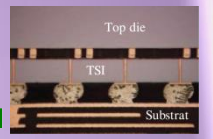
II. Fan-Out WLP





III. 2.5D IC





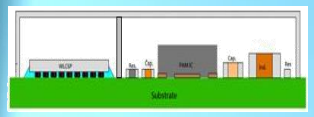
HOT !!

Product Features:

- *Small form factor with high function integration*
- *Higher performance (Electrical/Thermal/Mechanical)*
- *High C/P ratio (High valve, but low cost)*

Innovative 3D-SiP Package Solutions

SiP(System in PKG)



2.5D IC

Fan-Out WLP

3D-SiP Benefits & Challenges

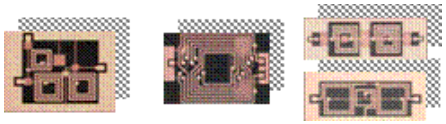
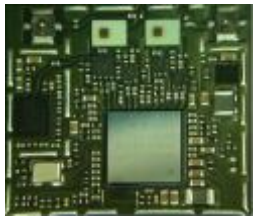
Application:

WiFi/ BT/ NFC / GPS / FM Module Development

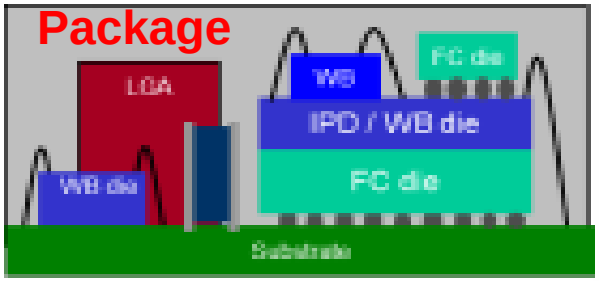



Benefits:

SiP can provide the ***small form factor***, ***low cost*** and ***multi-function integration*** solutions.

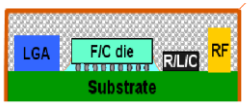
PCB

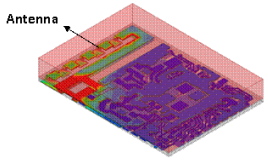


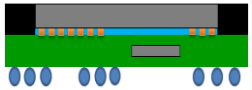
Challenges:

Some KEY technologies are needed to develop ASAP !!!

1. *EMI shielding*
2. *Antenna on PCB*
3. *Die on passive component*
4. *IPD/Die embedded in PCB*







3D-SiP Miniaturization Tech Solutions

75% size reduction

MCU + WiFi COB Solution

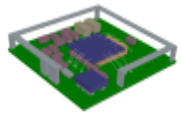
Size : 22x19mm

MCU + WiFi SiP solution

Size : 10x10mm

- **Include WiFi + MCU**
- **Component Count : 50**
- **Process : wafer thinning, stack Die on FC , MUF, EMI Coating**

80% size reduction



MCU + BLE COB Solution

Size : 18x12mm

MCU + BLE SiP solution

Size : 6.5x6.5mm

- **Include BLE, Flash, X'tal, Antenna**
- **Component Count : 28**
- **Process : Stack die on Passives, Antenna in Package, Compress Molding**

WiFi Plug

WiFi Air Conditioner

WiFi Bulb

BLE Locker

BLE Toy

iRhytm

WiFi Speaker

WiFi Sensor Hub

Hearing Aid

Swimming Band

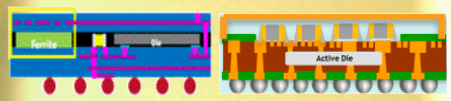
Hand Band

Innovative PKG Technologies for 3D-SiP

SPIL Leading

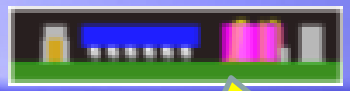
1.Embedded Actives

- Small PKG Size/Height



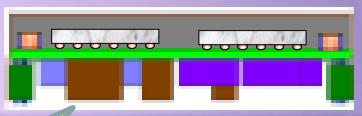
2.Embedded Passives

- Lower PKG Z Ht /
- Lower Power Consumption
- Low EMI Noise



3.Two side PKG

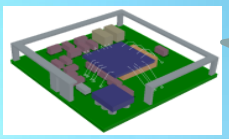
- High Yield /
- High Integration



Its Happen Now !!

7.Antenna in SiP

- Small PKG Size



.IPD on Die (F2F)

- Electrical Performance

6.Partition LMI

- Small Form Factor/ High Integration

5.Die on CAP

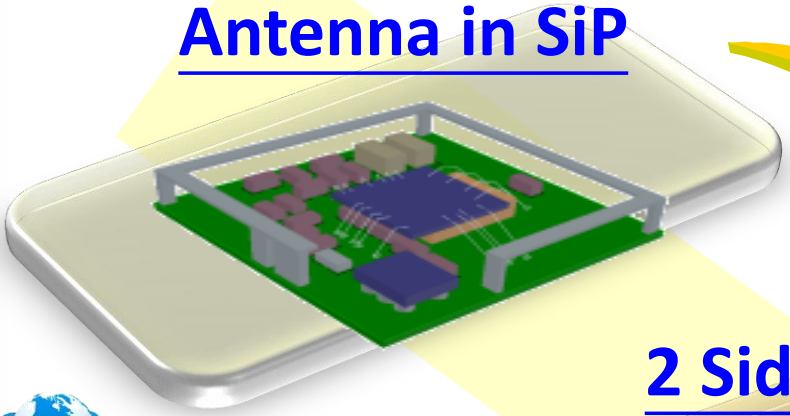
- Small PKG Size

1

3D-SiP New Package TECH. Trend

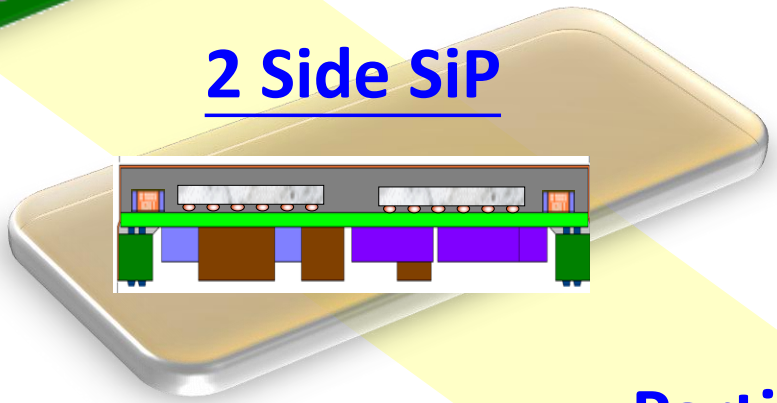
(CAGR →39.3% / 55.8%)

Antenna in SiP



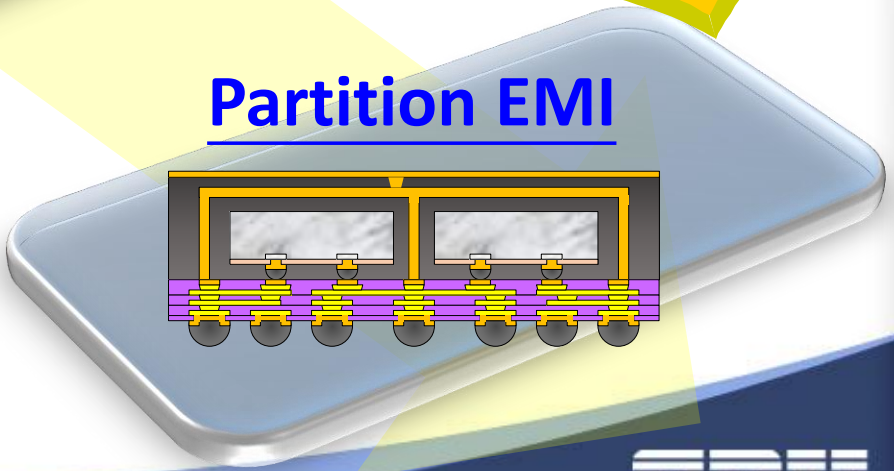
NOW!!

2 Side SiP



Next Generation!!

Partition EMI



Benefit :

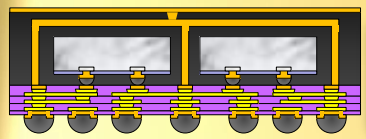
1. High function Integration
2. Small form Profile Performance

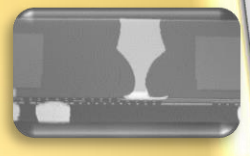
Innovative 3D-SiP Package Solutions

SiP(System in PKG)

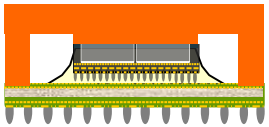
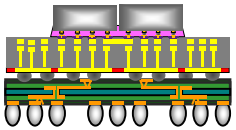
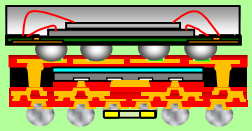
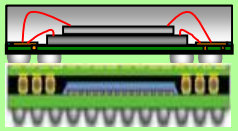
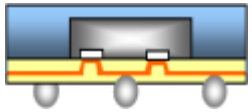
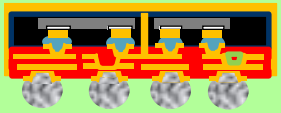
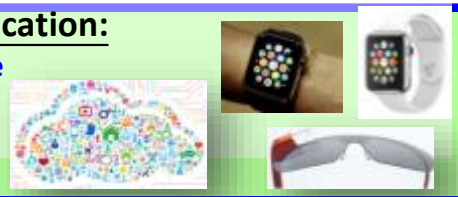
2.5D IC

Fan-Out WLP





FO-WLP PKG Category & Its Product Applications

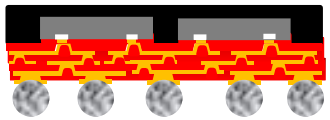
I/O Density	RDL L/S(um)	PKG Solution	Application
G1 Ultra High	0.1 ↓ 2	FO-MCM  Silicon Interposer 	**Networking Application:** 1. High performance computing 2. Networking 3. Data servers 
G2 High	2 ↓ 10	FO-PoP  HBW-PoP 	**Mobile Application:** 1. Smart Phone & Tablet 2. High End AP/BB 
G3 Low	>10	FO-SD  FC-ETS 	**Mobile Application:** 1. Low Pin Count 2. PMIC/RF/PA
G4 Middle	variability	FO-SIP  SIP Module 	**IoT/Wearable Application:** 1. Connectivity module 2. PMIC Module 

➢ *FO technology to fulfill potential product applications.*

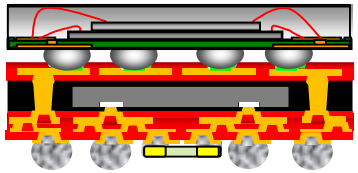
Why Fan-Out WLP Technology?

Application:

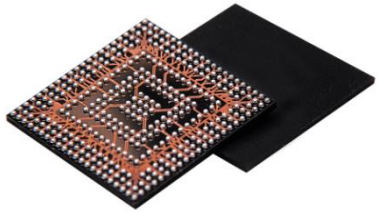
Keep sufficient area for PCB board I/O as the die size shrinking (28/20/16nm), application for Mobile AP/ Baseband/ PMIC and HDD/SSD Controller.



MCM-FOWLP

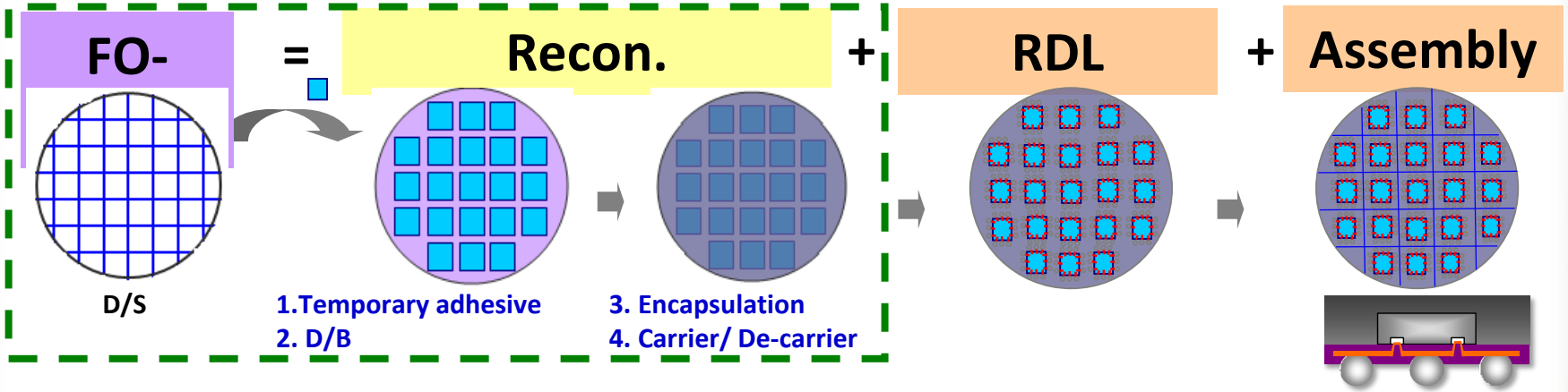


2sides RDL FO-PoP



Benefits:

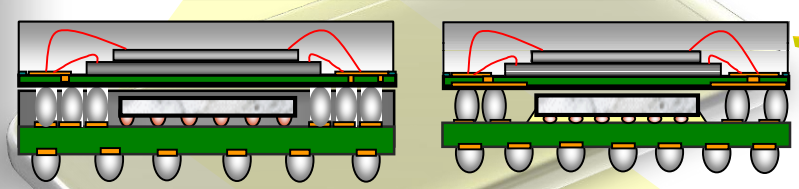
- ✓ Small form factor & thinner package (substrate-less).
- ✓ High IO/High bandwidth with fine line/multi-layer RDL routiability. (Line/Space = <10um, >2L RDL layer)



Challenges: ***Wafer Warpage &*** ***Poor BLR (Board Level Reliability)***

2 3D-SiP Package Apply for AP/BB in Smart Phone

ePoP & BD-PoP



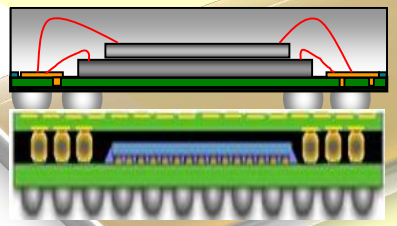
PKG THK: 1.2~1.5mm

PKG THK: 1.2mm

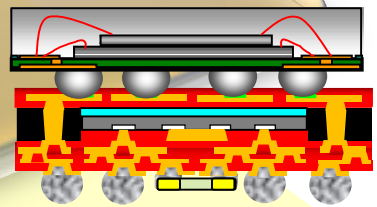
NOW!!

HWB-PoP & FO-PoP

(High Bandwidth)



PKG THK: <1.2mm

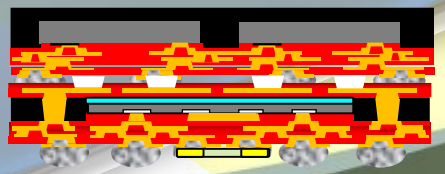


PKG THK: <1.1mm

Next Generation!!

FO-PoP+FO-MCM

(Ultra Thin Profile)



(Z ht <0.5mm)

PKG THK < 1mm

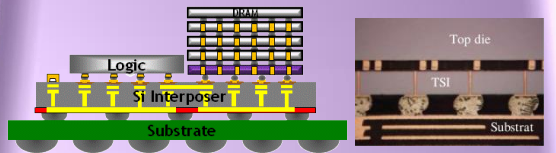
Benefit :

1. High Electric & Thermal Performance
2. Ultra thin Profile Performance

Innovative 3D-SiP Package Solutions

SiP(System in PKG)

2.5D IC

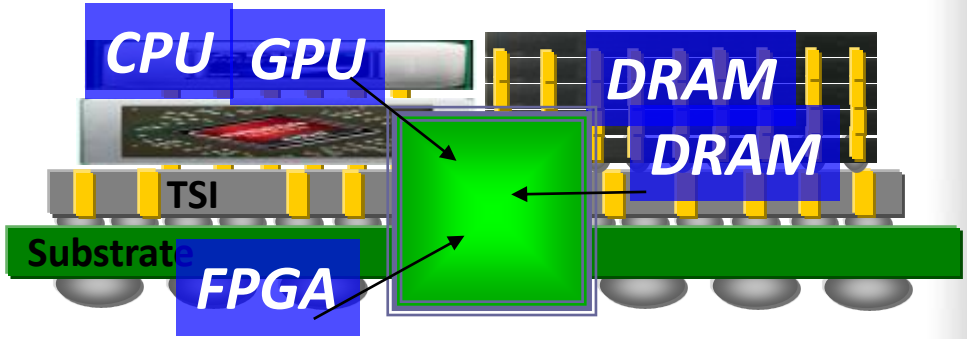


Fan-Out WLP

Why 2.5DIC Technology?

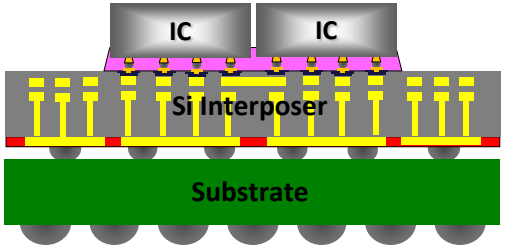
AI Market
(deep learning, supercomputer)

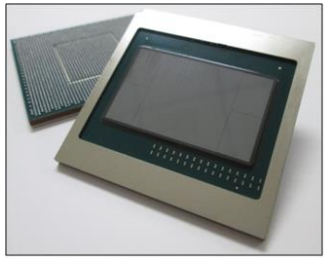
The Trend of Future!



- ✓ Heterogeneous integration
- ✓ Smaller PKG size
- ✓ Higher performance

OSAT Role in 2.5DIC Supply Chain

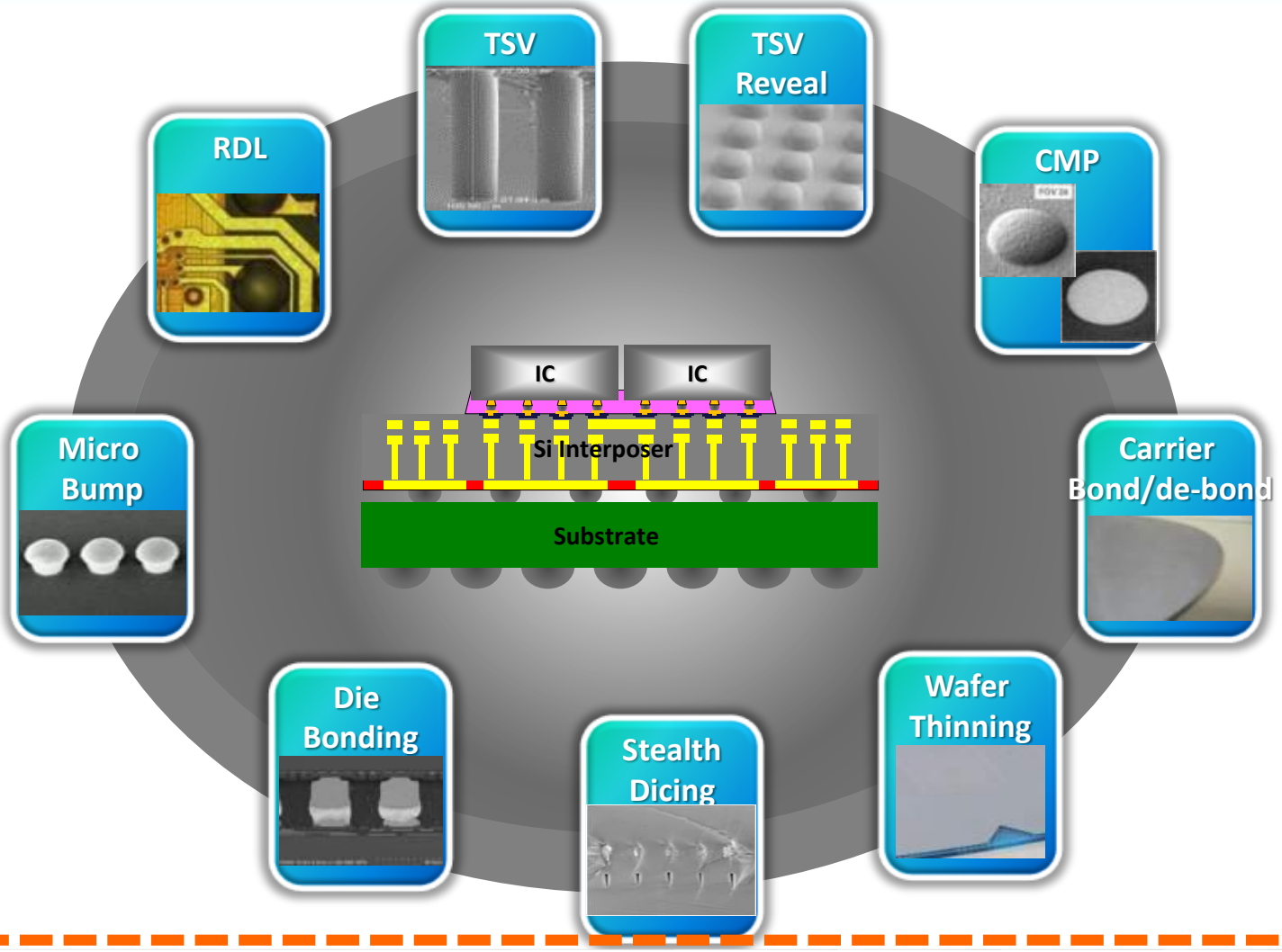




Process / Model	FEoL		MEoL		BEoL		
	Logic IC	TSV + FS RDL	Front-side Micro-pad	Backside Via Reveal	BS RDL + Bump	Micro Joint & Assembly	Test
2.5D	IC Fab		SPIL				
3D	IC Fab		SPIL				

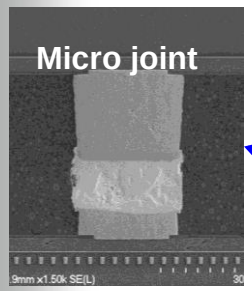
- *Enabling technologies development for 2.5DIC MEoL and BEoL capability. Same capability capable for 3DIC.*
- *For TSV Silicon Interposer (TSI), OSAT collaborate with wafer foundries*

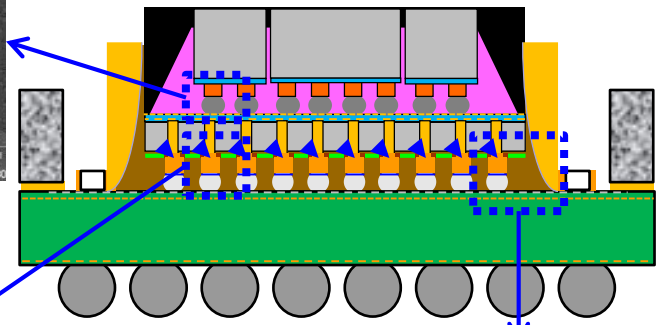
2.5DIC Key Enabling Technology

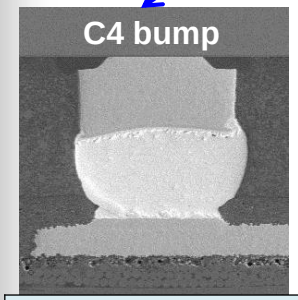


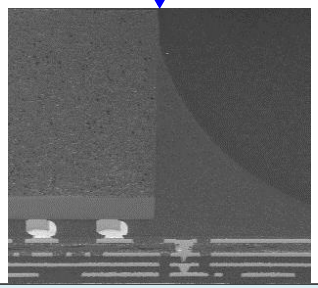
Challenges: Wafer Warpage & Poor PLR(Package Level Reliability)

2.5D Packaging Readiness

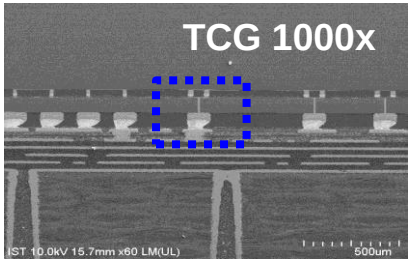


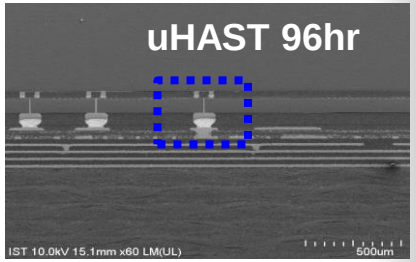


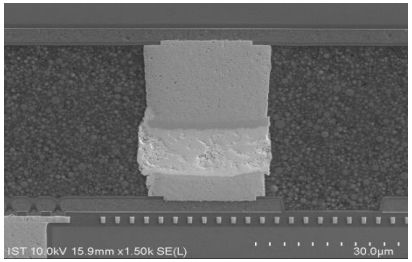


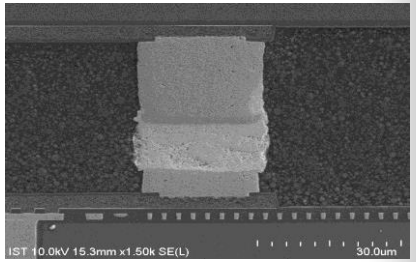


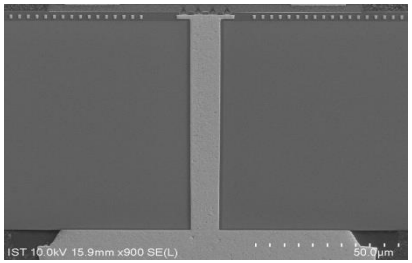
X-section check		
Precon (L4/ reflow 245℃)	**RFL 3x**	**Pass**
TCG (-40~125C)	**1000x**	**Pass**
uHAST (Ta=130℃/RH 85%)	**96hr**	**Pass**

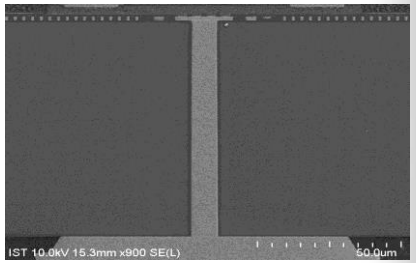


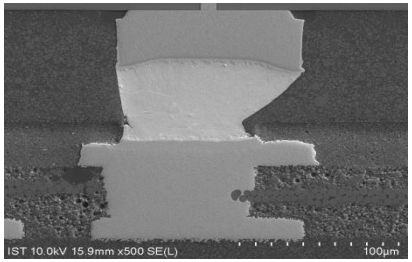


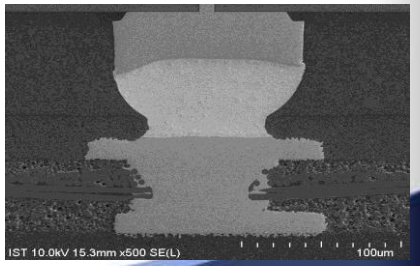






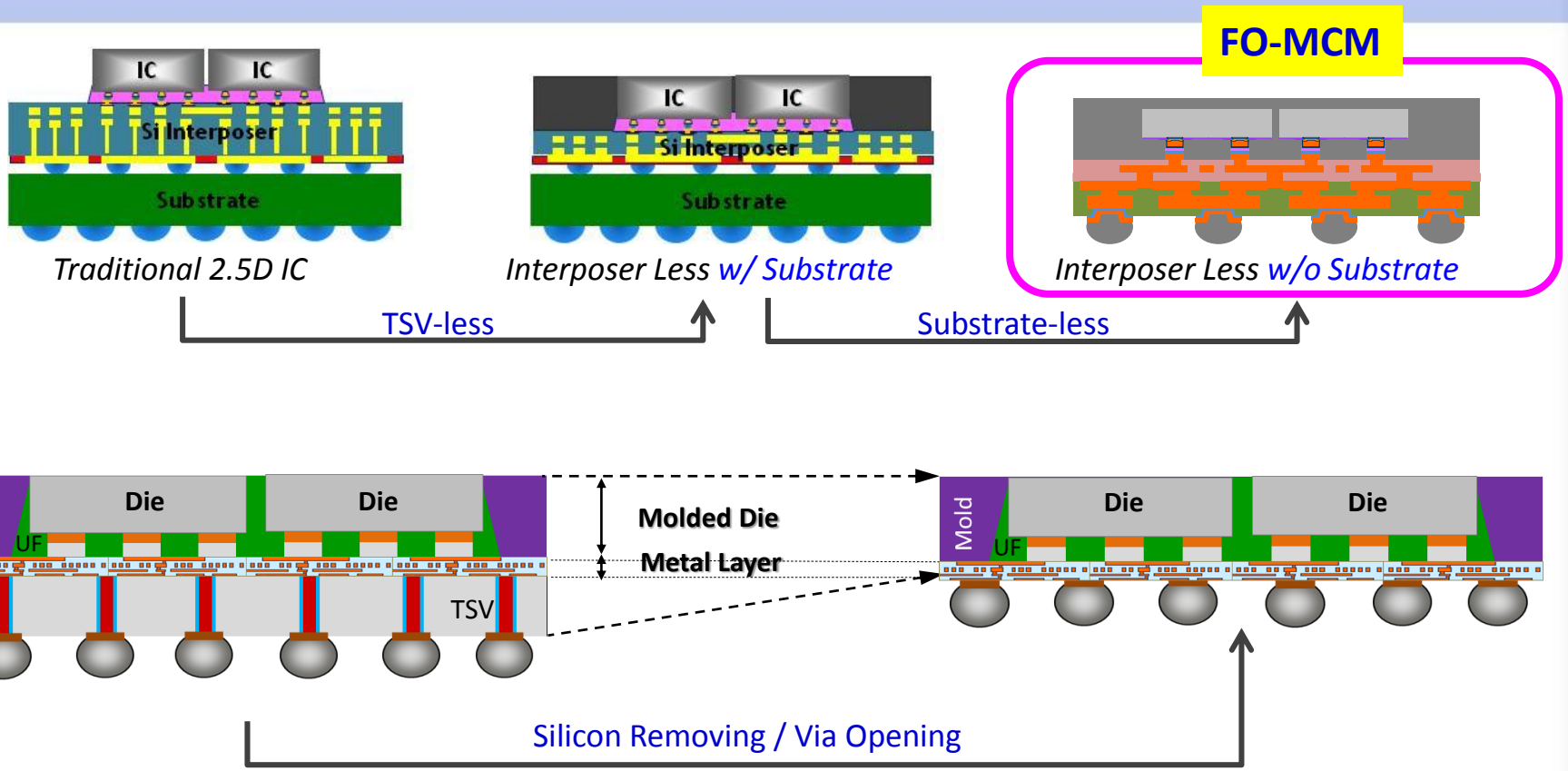






- ✓ **No abnormal was observed on C4 bump joint , UF dispense and adhesive process**
- ✓ **1 ASIC +4HBM structure passed L4 + TCG1000**

FO-MCM (w/o Si Interposer) - Low Cost Alternatives of 2.5D

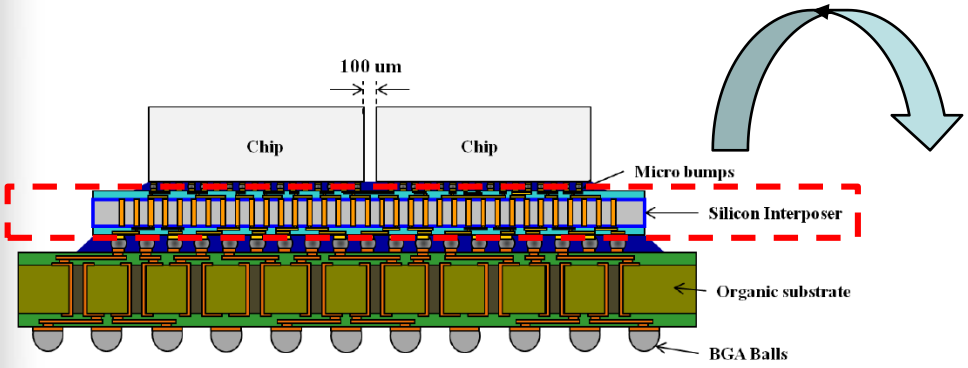


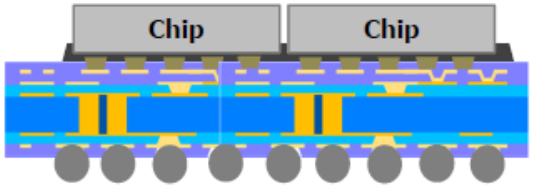
✓ *Merits of **2.5D IC to FO-MCM Platform***

- *Shortening interconnection distance - high speed & bandwidth performance.*
- *Reducing interposer cost due to excluding TSV related process cost.*
- ***Processing by all existing MEoL/BEoL equipments.***

2.1D (by Substrate) - Low Cost Alternatives of 2.5D

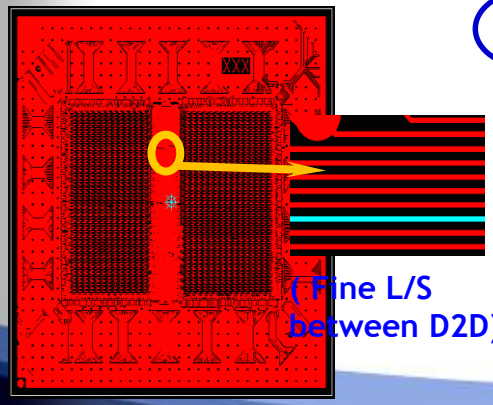
- Organic Interposer: (w/ core)





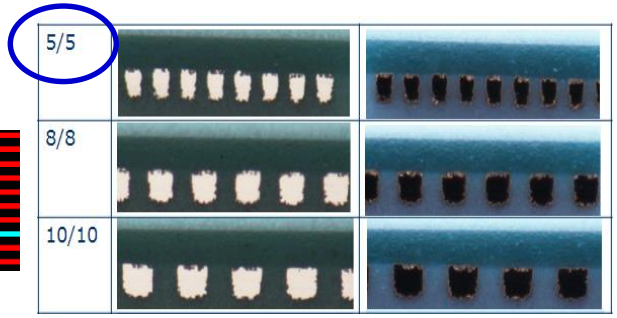
- Organic Substrate replace Si interposer as interface between die & substrate.
- Characteristic:
  - Fine pitch: trace L/S >>10/10 → 2/2um

- Fine L/S capacity

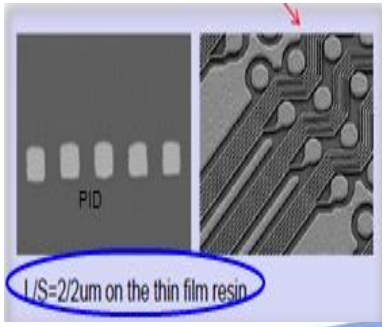


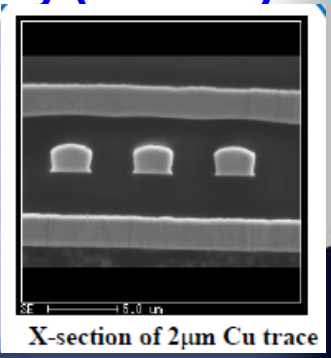
(Fine L/S between D2D)

2014 capability (L/S=5/5)



2016 capability (L/S=2/2)





X-section of 2μm Cu trace

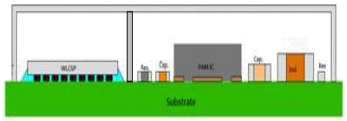
Outline

- *Packaging Trend of SMART Phone/Wearable/ Networking Devices*
- *Innovative 3D-SiP Packaging Technologies*
- ***Summary***

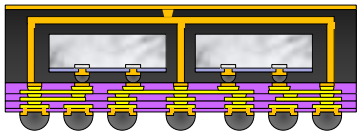
Conclusion

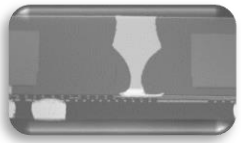
- ***New Package TECHs Focuse on Three 3D-SiP***

  - ***System in Package*** ***(w/ 7 miniaturization TECH)***

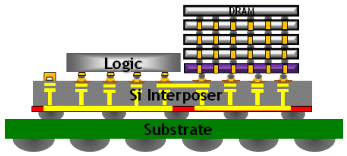


  - ***Fan-Out Wafer Level Package*** ***(Substrate-less; for thin & small form factor)***





  - ***2.5DIC PKG*** ***(w/ Low Cost PKG solutions; such as 2.1D Substrate)***



Thank You For Your Attention!!!

Contact Information:

albertlan@spil.com.tw

藍章益