Memory Packaging Challenges for the New Era

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- TRACK INNOVATION
- IDENTIFY TRENDS
- ANALYZE GROWTH
- INFLUENCE DECISIONS

RELEVANT, ACCURATE, TIMELY
Outline

• Mobile memory packaging trends
• Wearable electronics
• SSD trends and new non-volatile memory
• Memory for automotive safety features
• High-performance memory packaging trends
• China joins the memory club
Demand for Thin Smartphones Drives Package Developments

- Smartphones volumes remain largest volume application in units
  - Approximately 1.5 billion
  - IDC predicts smartphone volumes will increase by 4.2% this year
  - Mobile devices drive demand for DRAM and flash
- Smartphones drive thinner packages
  - Low profile requirements for thin product and to create more room for battery
  - New forms of package-on-package (PoP)

Separate package for logic
Separate package for memory
Packages individually tested, then stacked
Qualcomm MDM9645M LTE X12 Modem

- Modem chip is flip chip bonded to substrate
- Memory wire bonding on top

Package size: 8.41 mm x 8.61 mm x 0.71 mm
Modem chip: 6.14 mm x 5.45 mm x 0.098 mm
Memory: 4.38 mm x 3.7 mm x 0.072 mm

Source: TPSS.
Application Processor and Memory Packaging Trends

• Thinner package and smaller footprint
  – High-end smartphone ≤0.8mm package height

• 3D IC with TSV provides the ultimate in package height reduction, but continues to be pushed out (thermal, cost, business issues)

• PoP in high-end smartphones
  – Option 1: Continue with FC on thin substrate
  – Option 2: Embedded AP in bottom laminate substrate
  – Option 3: Fan-out WLP with application processor as bottom package and memory in top package
  – Option 4: Some new format (RDL first/chip last)

• Challenge is memory top package moving to finer ball pitch for packages
  – Requires pre-stack of memory on AP package

• FO-WLP AP in bottom PoP for Apple’s A10 processor
  – Low profile
  – High routing density
  – Improved electrical and thermal performance

InFO is 20% thinner than FC-PoP
3D IC Design: Thermal is Critical

- Low-cost thermal management solutions required for logic and memory stacking
- Current PoP solution provides better thermal solution
- Thermal issues: 3D circuits increase total power generated per unit surface area
  - Chips in the stack may overheat if cooling is not provided
  - Space may be too small for cooling channels (very small gap for fluid flow)
  - Thinning chips creates extreme conditions for on-chip hot spot
  - Need new low-power designs

Source: Renesas.
Trends for Top PoP Memory Package

- Package-on-package (PoP) made up of logic in bottom package and memory (typically >1 die) in top package
- Apple A10 PoP includes FO-WLP for bottom package, four side-by-side memory wire bonded on laminate substrate for top PoP
- Future versions of top memory package could use FO-WLP

Source: eWiseTech.
Amkor’s SWIFT™ High Yield FO-WLP with Chip Last

- **Target applications**
  - Mobile
  - Networking

- **Target device types**
  - Baseband
  - Application processor
  - Logic + memory

- **Utilizes existing bump and assembly capability**
  - Multi-die and large die capability as well as large package body size
  - 3D format possible by stacking packages with Cu pillars or through molded via (TMV)

Source: Amkor.
Google’s View of Future Memory Requirements

- Need an affordable DRAM-based IPM closely coupled to an application processor with low voltage swing I/O in FO-WLP
  - Allows fine-pitch RDL routing and short distance between AP die and IPM
  - Increases interconnect bandwidth dramatically from number of pin outs and data rate perspective
  - Termination-less low voltage I/O swing I/O transceiver/receiver circuits ideal for within package chip-to-chip communication
  - Allow aggressive reduction in signal swing for power optimization because the data bus inversion and reduce trace distance

In Package Memory Concept

LVSIO : Low Voltage Swing IO
LPDDR4 : Low Power Double-Data-Rate
TSV : Through Silicon Via
FOWLP : Fan-out Wafer Level Package
POP : Package on Package
Wearables

- Health and fitness tracking bands including pedometers
- Watch products
- System-in-Package (SiP) modules include
  - Connectivity
  - Controller
  - Memory (Flash, SRAM, etc.)
  - MEMS

Source: Apple..
Packages in Apple Watch Module

- **Stacked die CSP for processor and memory packaging**
  - Package height 0.56 mm
  - Processor solder bumped flip chip
  - Memory wire bond
- **NAND flash memory stacked die CSP**
  - Package height ~0.60 mm

Stacked die CSP (logic bottom die, memory top die)

Source: TPSS.
Solid-State Drives Fueling Flash Demand

- **External and Add-in Card SSD:**
  - 1TB is popular high-capacity drive
  - Largest 2.5-inch drive in production is 16TB; 24TB and 32TB in future

- **Embedded SSD (microSSD):**
  - Up to 512GB in a single 16 mm x 20 mm BGA

- **Boards or cards:**
  - Single- or double-sided
  - Generally have 1 to 8 NAND packages; Enterprise boards have as many as 32-40
  - High-speed SSDs can also have a DRAM on board for caching

**Micron 2.4TB PCIe Enterprise SSD:**
- 32 x 16nm MLC NAND (16 on each side)
- 1 x NVMe 16-channel controller
- 9 x 512Mb DRAM (5 on one side, 4 on other)

**Samsung 512GB BGA SSD:**
- 16 x 48-layer MLC V-NAND (256Gb/die)
- 1 x ARM-based controller
- 1 x LPDDR4: 4Gb

Source: Samsung, Anandtech.

Source: Storage Review.
Flash Memory Stack

• **3D Flash memory packaging**
  – Wire bond for most cost effective solution
  – Everyone has a TSV demonstration vehicle
  – Cost has limited HVM application of flash with TSV stack some low-volume production expected to start this year for SSD

• **Semiconductor process with stacked cells**
• **New semiconductor non-volatile memory development**
Advanced Driver Assistance Systems (ADAS)

- From increasing number of safety features to autonomous driving......
- Drives increased use of sensors including CMOS image sensor for camera modules, collision sensors, object detection, etc.
- Increased processing capability
- System design and co-design
- Memory as part of system-in-package (SiP) module
  - Flash
  - Serial EEPROM
- Challenge is harsh reliability requirements for automotive environment
Block Diagram of Infineon SP37 Tire Pressure Sensor

Source: Infineon.
NXP CONNECTS THE CAR - SMART RECEPTION & SENSING

Supported by automotive qualified Transistors, Diodes, Power MOSFETs and Logic devices.
Renesas Module Sensor Fusion/ADAS Control ECU

- Results from radar and camera sensors are fused with vehicle acceleration, braking, and handling systems to avoid and reduce the possibility of accident in advance
- Modules include memory such as EEPROM
- Future systems other applications may use high bandwidth memory (HBM)
High Performance Memory Stacks with TSV

- **New memory architectures**
- **Tezzaron high-speed memory**
  - Production shipments
  - High-performance applications
- **Micron Hybrid Memory Cube (HMC)**
  - Intel’s Knight’s Landing
- **Samsung**
  - DIMMS for servers
  - HBM (DRAM) stacks with TSVs
- **SK Hynix**
  - HBM on silicon interposer for GPU
  - Advantages include higher bandwidth, lower latency, and lower power consumption

Source: Samsung.
Source: SK Hynix.
Source: Micron.
Samsung’s DDR4 with TSV

- Samsung’s 128GB RDIMM uses DDR4 memory with TSVs
  - DDR4 DRAMs fabricated on 20nm silicon node technology
- Targeted for Datacenters and Servers
  - Lower power
  - Double capacity of originally 64GB LRDIMM developed for Enterprise servers
Lower Power Consumption

- Lower Cio (0.4pF) and no termination...small I/O current consumption
- Lower speed per pin (1Gbps)... low power consumption

Source: SK Hynix.
AMD’s “Fiji” with Silicon Interposer with TSVs

**ASIC**
- Large die size: 586 mm²
- Fine pitch: ~40 μm
- High bump count: >200 k

**Si Interposer**
- Huge die size: 36 mm x 28 mm
- High pad count
- High C4 count: >20 k
- TSVs: 65 k; 10 μm diameter

**High Bandwidth Memory (HBM)**
- Die size: 5 x 7 mm
- High bump density: ~5 k
- Small UBM: 25 μm
- Stacked dies: 4 DRAM + 1 Logic

**Package**
- Organic BGA substrate
- Size: 55 mm x 55 mm

- AMD’s graphics processor uses silicon interposer with TSVs
- More than 200,000 interconnects in the module including Cu pillar μbumps and C4 bumps
- Interposer has 65,000 TSVs with 10μm diameter vias
AMD’s “Fiji” with Silicon Interposer and HBM

- AMD “Fiji” solution for the graphics market
- Four HBM stacks, each containing stacked DRAMs and a logic die with TSVs mounted on the interposer

Source: AMD.
Xilinx Products with Silicon Interposer

- Future products with HBM
- Silicon interposer to handle communication between HBM stack and FPGA

Source: Xilinx.
Developing a Strong Memory Industry: Management Matters

- Memory industry continues to move around the globe
  - US
  - Japan
  - Korea
  - Taiwan
  - China

- Development of memory industry requires more than just technology
- Packaging developments will be key to memory success
Conclusions

• Mobile devices (smartphones) drive unit volumes
  – Mobile DRAM
  – Flash memory
• Growth of SSDs driving flash memory volume growth
• New non-volatile memory developments
• High performance computing lower volumes, but increasing use of high-performance memory with TSVs
  – DIMMs with TSV for increasing number of applications
  – HBM on interposers
  – Performance is important, but cost is not irrelevant
  – Companies working on methods to lower cost of HBM
• Memory industry continues to evolve
Thank you!

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