

Memory Industry Updates

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Worldwide Semiconductor Business Update

- The worldwide semiconductor market was up 1.1% in 2016 to US\$338.9 Billion
- The year 2017 is forecasted to be strong with 6.5% growth to US\$361 billion
- The memory is forecasted to be 12.8% growth to US\$86.6 billion in 2017
- 2018 is forecasted to be up another 2.3% to **US\$369** billion
- In 2017, the largest growth is expected across sensors, analog, and memory
- All regions are forecasted to return to growth in 2017 as well

| Autumn 2016 - Q4 update | Amounts in US\$M | | | | Year on Year Growth in % | | | |
|--------------------------|------------------|---------|---------|---------|--------------------------|------|------|------|
| Autumii 2016 - Q4 upuate | 2015 | 2016 | 2017 | 2018 | 2015 | 2016 | 2017 | 2018 |
| Americas | 68,738 | 65,537 | 72,173 | 74,102 | -0.8 | -4.7 | 10.1 | 2.7 |
| Europe | 34,258 | 32,707 | 33,892 | 34,636 | -8.5 | -4.5 | 3.6 | 2.2 |
| Japan | 31,102 | 32,292 | 33,608 | 34,200 | -10.7 | 3.8 | 4.1 | 1.8 |
| Asia Pacific | 201,070 | 208,395 | 221,230 | 226,113 | 3.5 | 3.6 | 6.2 | 2.2 |
| Total World - \$M | 335,168 | 338,931 | 360,903 | 369,050 | -0.2 | 1.1 | 6.5 | 2.3 |
| Discrete Semiconductors | 18,612 | 19,418 | 20,023 | 20,674 | -7.7 | 4.3 | 3.1 | 3.2 |
| Optoelectronics | 33,256 | 31,994 | 32,679 | 32,241 | 11.3 | -3.8 | 2.1 | -1.3 |
| Sensors | 8,816 | 10,821 | 11,797 | 12,394 | 3.7 | 22.7 | 9.0 | 5.1 |
| Integrated Circuits | 274,484 | 276,698 | 296,404 | 303,741 | -1.0 | 0.8 | 7.1 | 2.5 |
| Analog | 45,228 | 47,848 | 51,570 | 53,315 | 1.9 | 5.8 | 7.8 | 3.4 |
| Micro | 61,298 | 60,585 | 61,106 | 62,281 | -1.2 | -1.2 | 0.9 | 1.9 |
| Logic | 90,753 | 91,498 | 97,154 | 98,975 | -1.0 | 0.8 | 6.2 | 1.9 |
| Memory | 77,205 | 76,767 | 86,574 | 89,170 | -2.6 | -0.6 | 12.8 | 3.0 |
| Total Products - \$M | 335,168 | 338,931 | 360,903 | 369,050 | -0.2 | 1.1 | 6.5 | 2.3 |





2017F Major Capital Spenders

| Company | 2015 (\$M) | 2016 (\$M) | 16/15 % Change | 2017F (\$M) | 17/16 % Change |
|--------------------|---|--|--|--|---|
| Samsung | 13,010 | 11,300 | -13% | 12,500 | 11% |
| Intel | 7,326 | 9,625 | 31% | 12,000 | 25% |
| TSMC* | 8,089 | 10,249 | 27% | 10,000 | -2% |
| SK Hynix | 6,011 | 5,188 | -14% | 6,000 | 16% |
| Micron** | 4,500 | 5,760 | 28% | 5,000 | -13% |
| SMIC* | 1,401 | 2,626 | 87% | 2,300 | -12% |
| UMC* | 1,899 | 2,842 | 50% | 2,000 | -30% |
| GlobalFoundries* | 3,985 | 1,500 | -62% | 2,000 | 33% |
| Toshiba | 1,745 | 1,840 | 5% | 1,900 | 3% |
| SanDisk/WD | 1,460 | 1,750 | 20% | 1,800 | 3% |
| ST | 467 | 607 | 30% | 1,050 | 73% |
| Top 11 Total | 49,893 | 53,287 | 7% | 56,550 | 6% |
| Others | 15,339 | 14,695 | -4% | 15,755 | 7% |
| Total Cap Spending | 65,232 | 67,982 | 4% | 72,305 | 6% |
| | Samsung Intel TSMC* SK Hynix Micron** SMIC* UMC* GlobalFoundries* Toshiba SanDisk/WD ST Top 11 Total Others | Company (\$M) Samsung 13,010 Intel 7,326 TSMC* 8,089 SK Hynix 6,011 Micron** 4,500 SMIC* 1,401 UMC* 1,899 GlobalFoundries* 3,985 Toshiba 1,745 SanDisk/WD 1,460 ST 467 Top 11 Total 49,893 Others 15,339 | Company (\$M) (\$M) Samsung 13,010 11,300 Intel 7,326 9,625 TSMC* 8,089 10,249 SK Hynix 6,011 5,188 Micron** 4,500 5,760 SMIC* 1,401 2,626 UMC* 1,899 2,842 GlobalFoundries* 3,985 1,500 Toshiba 1,745 1,840 SanDisk/WD 1,460 1,750 ST 467 607 Top 11 Total 49,893 53,287 Others 15,339 14,695 | Company (\$M) (\$M) Change Samsung 13,010 11,300 -13% Intel 7,326 9,625 31% TSMC* 8,089 10,249 27% SK Hynix 6,011 5,188 -14% Micron** 4,500 5,760 28% SMIC* 1,401 2,626 87% UMC* 1,899 2,842 50% GlobalFoundries* 3,985 1,500 -62% Toshiba 1,745 1,840 5% SanDisk/WD 1,460 1,750 20% ST 467 607 30% Top 11 Total 49,893 53,287 7% Others 15,339 14,695 -4% | Company (\$M) (\$M) Change (\$M) Samsung 13,010 11,300 -13% 12,500 Intel 7,326 9,625 31% 12,000 TSMC* 8,089 10,249 27% 10,000 SK Hynix 6,011 5,188 -14% 6,000 Micron** 4,500 5,760 28% 5,000 SMIC* 1,401 2,626 87% 2,300 UMC* 1,899 2,842 50% 2,000 GlobalFoundries* 3,985 1,500 -62% 2,000 Toshiba 1,745 1,840 5% 1,900 SanDisk/WD 1,460 1,750 20% 1,800 ST 467 607 30% 1,050 Top 11 Total 49,893 53,287 7% 56,550 Others 15,339 14,695 -4% 15,755 |

^{*}Pure-Play Foundry

Source: IC Insights, Company Reports

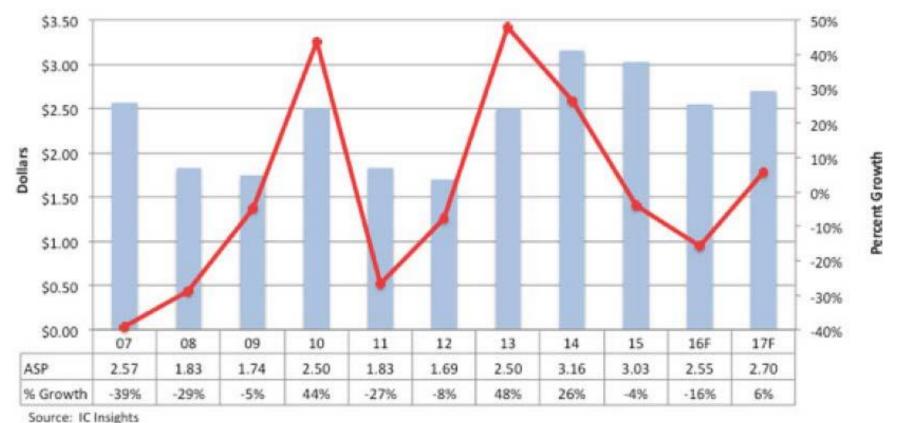


^{**} Includes Inotera in 2017.

Volatile DRAM ASP Growth



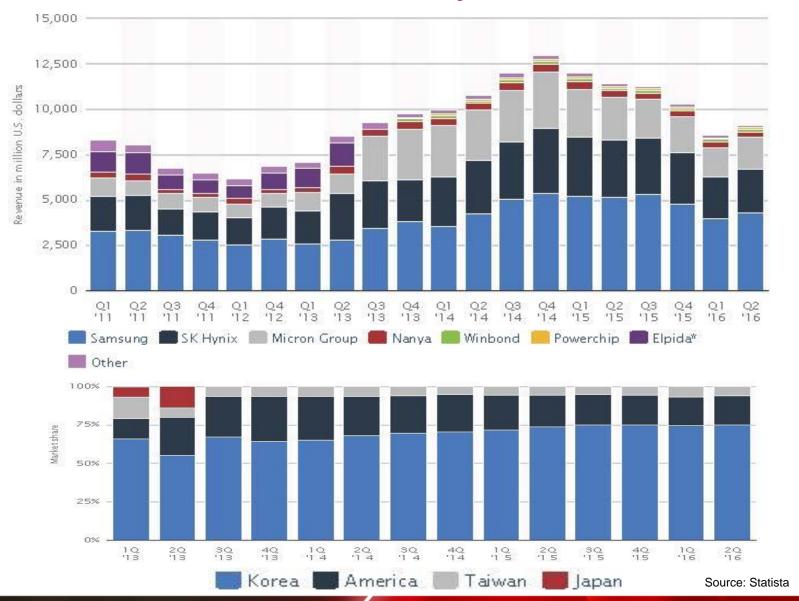
- DRAM ASPs started to strengthen in the late 2nd quarter of 2016, and expected to continue increasing into 2017
- The boost to DRAM ASP is expected to come from demand for enterprise (server) systems due to the need to process "big data"
- Low-voltage DRAM continues to enjoy solid demand for use in mobile platforms





Global DRAM Revenue by Manufacturers









DRAM Development Trend

Memory Technologies have been and will always be the drivers of Moore's Law

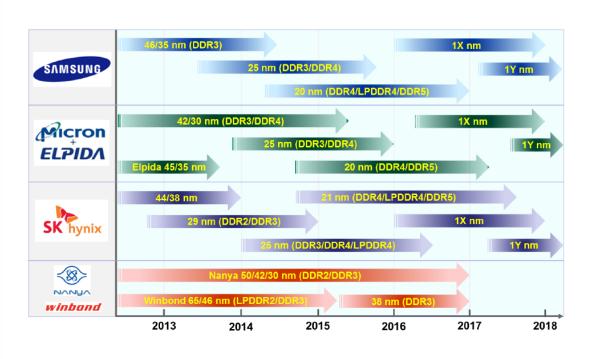
Beyond 20nm, the DRAM is expected to scale:

<u>1xnm: 16nm ~ 19nm;</u> <u>1ynm: 14nm ~ 16nm;</u> <u>1znm: 12nm ~ 14nm</u>

DRAM Technology Review

TECHINSIGHTS

■ DRAM Process Node Roadmap (Manufacturers)



DRAM Challenges

Satisfy Bandwidth requirements,

Reduce Power Consumption,

Maintain Low Cost



JEDEC is working on DDR5



• JEDEC specs for DDR5 will be released this year and sample will begin in 2018

| Spec Items Density / Speed | | DDR4 | DDR5 | | |
|----------------------------|-----------------------|--------------------------|--|--|--|
| | | 4Gb~16Gb / 1.6~3.2Gbps | 8Gb~64Gb / 3.2~6.4Gbps | | |
| Interface | Voltage(VDD/VDDQ/VPP) | 1.2V/1.2V/2.5V | 1.1V/1.1V/1.8V POD (TBD ohm) | | |
| | Data IO | POD (34ohm) | | | |
| | CA IO | RTT | CA ODT | | |
| Core | # of banks | 16Banks (4Bank Group) | 16Banks(8Gb)/32Banks(16+Gb) (8Bank Group) | | |
| | # prefetch | 8bits | 16bits | | |
| Physical | PKG(x4,x8/x16) | 78 / 96 BGA | 78 / 96 BGA (TBD) | | |
| | DIMM type | R, LR, U, So | Same as DDR4 | | |
| | DIMM Capacity | 4GB to 256GB | 8GB to 4TB | | |
| | # of DRAM / DIMM | 36 (Max) | 40 (Max) | | |
| | DIMM pins | 288 | 288 (target, TBD) | | |
| | Voltage regulator | On MB | VR on DIMM | | |
| Scaling features | | X | On-die ECC, tWR | | |

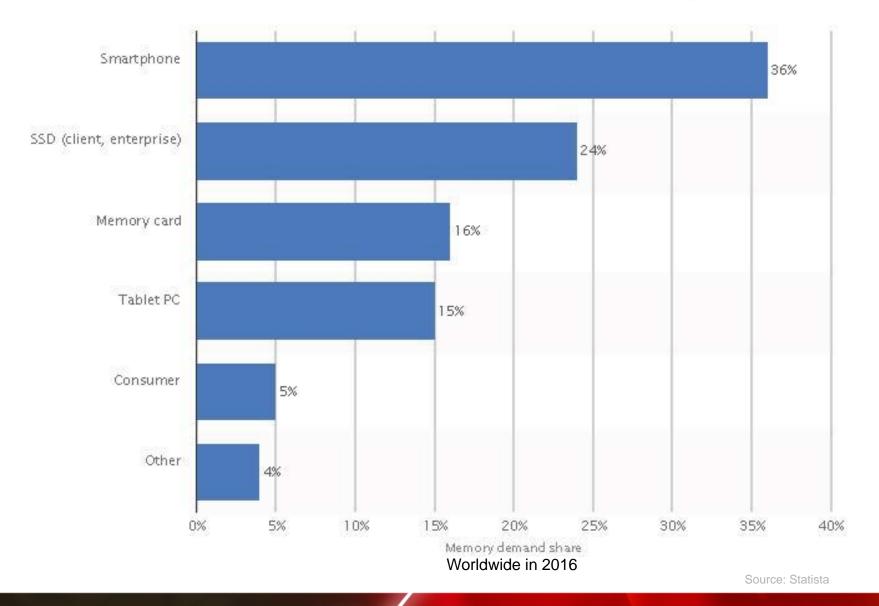
- Benefits of DDR5:
 - Cram more memory into PCs
 - Running apps faster
 - Denser than earlier DRAMs
 - Consume less power
- Servers will be the first to get DDR5, and it could reach desktops and laptops 12 to 18 months later

| DDR SDRAM Standard | Internal rate (MHz) | Bus clock (MHz) | Prefetch | Data rate (MT/s) | Transfer rate (GB/s) | Voltage (V) |
|-----------------------|---------------------|--------------------|----------|---------------------|-------------------------|----------------|
| SDRAM | 100-166 | 100-166 | 1n | 100-166 | 0.8-1.3 | 3.3 |
| DDR | 133-200 | 133-200 | 2n | 266-400 | 2.1-3.2 | 2.5/2.6 |
| DDR2 | 133-200 | 266-400 | 4n | 533-800 | 4.2-6.4 | 1.8 |
| DDR3 | 133-200 | 533-800 | 8n | 1066-1600 | 8.5-14.9 | 1.35/1.5 |
| DDR4 | 133-200 | 1066-1600 | 8n | 2133-3200 | 17-21.3 | 1.2 |



Distribution of NAND bits by device segment

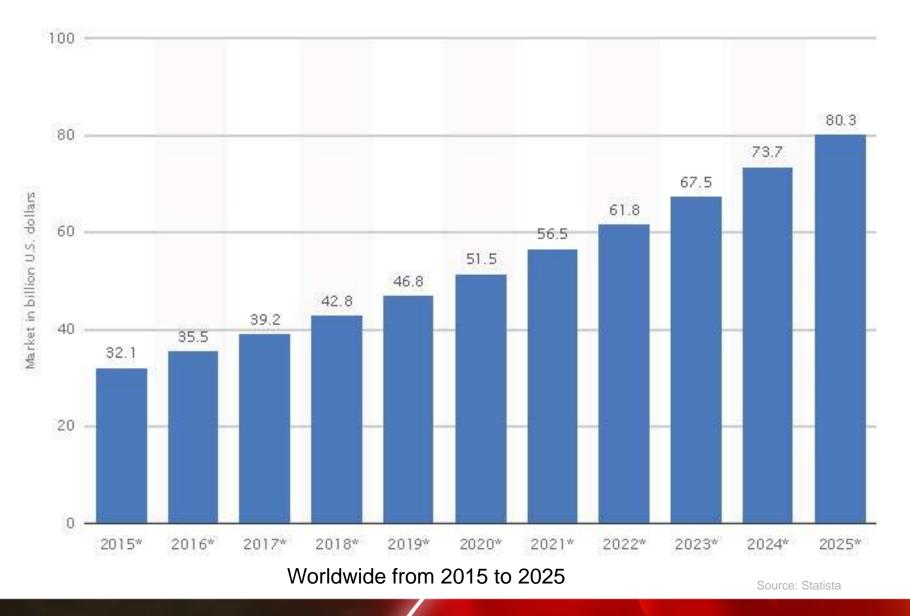






2D/3D NAND Flash Market Size





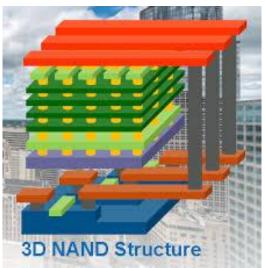


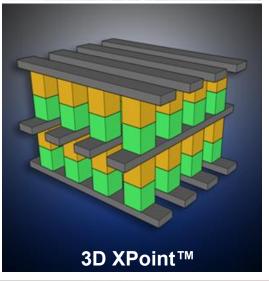
Advanced Flash Memory and Challenges



Innovative flash technologies: 3D NAND and 3D XPoint™









Stack deposition

- Wafer bow due to stress
- Layer-to-layer uniformity
- Defects



Memory Hole Etch

- Etch Selectivity to hardmask
- To-to-bottom CD uniformity
- Etch profile integrity for high aspect ratio



Wordline Fill

- Void-free fill of complex structures (vertically and horizontally)
- Stress induced wafer bow
- Defects due to fluorine attach



Stair Etch

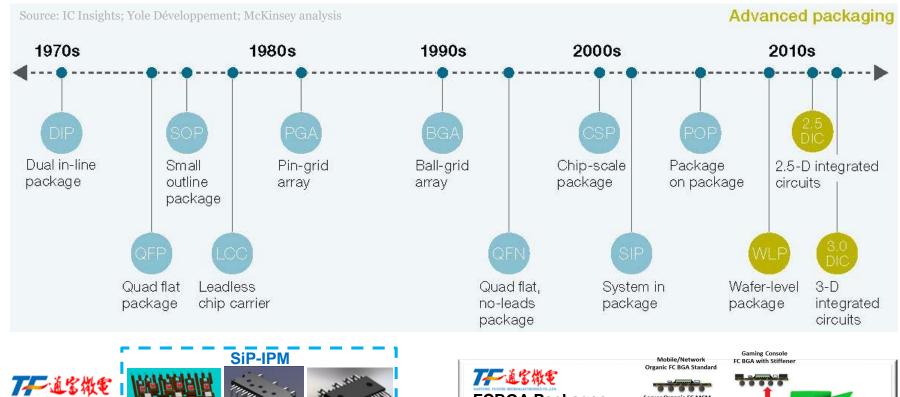
- Etch precision for repeatable stair CD
- Lateral/vertical selectivity (to photoresist)

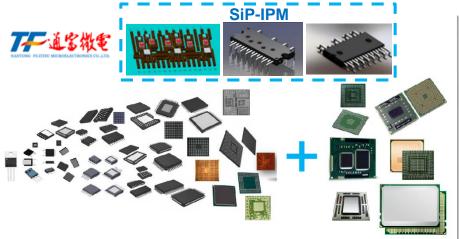
Source: LAM Research

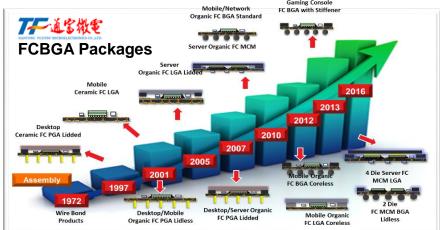


Electronic Packaging Evolution since the 1970s











Advanced Memory Packaging & Segments





Wire Bond Die Stacks

TSV Die Stacks



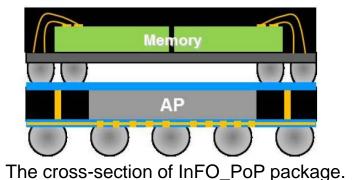


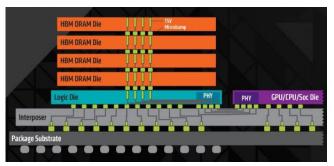




Notebook

Source: JEDEC





AMD HBM breaks the processing bottleneck

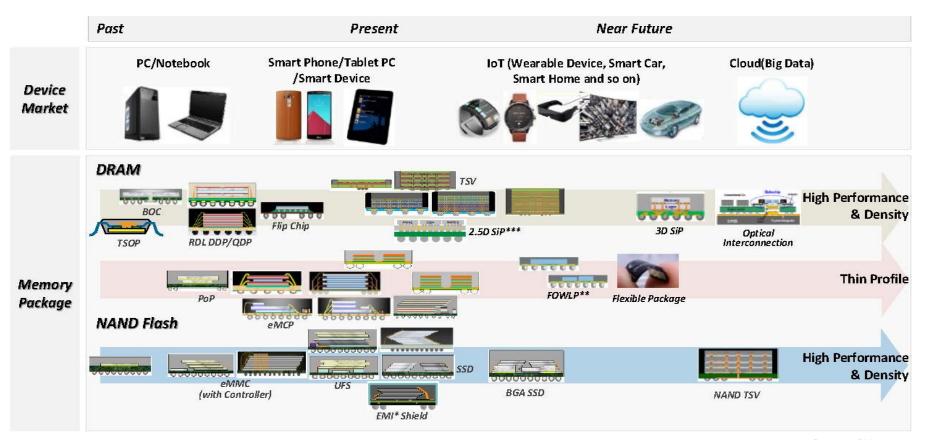


Global Standards for the Microelectronics Industry

Memory Packaging Roadmap



FC and TSV/WLCSP should satisfy faster speed, wider bandwidth and smaller/thinner



Source: SK htnix



China Developing Memories



Yangtze River Storage Technology (YRST)

- Acquired XMC
- 3D NAND, DRAM
- Beijing, Wuhan, Nanjing

Fujian Jin Hua Integrated Circuit

- Partner with UMC
- DRAM
- Quanzhou

GigaDevice Semiconductor

- Publiced at Shanghai Stock Exchange - <u>603986</u> (SHA)
- Acquired ISSI, a USA company
- NOR, NAND, SPI flash, DRAM. MCU
- Beijing

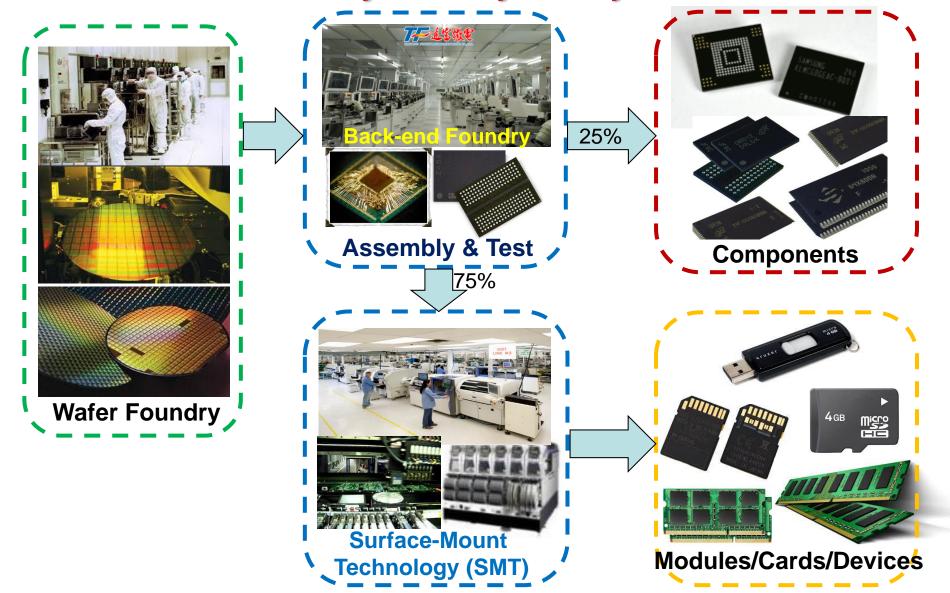


Source: EE Time



Memory Industry Eco-system





直管微電 NANTONG PUJITSU MICROELECTRONICS CO.,LTD.

JEDEC Encourages China Memory Makers Join Industry Leaders



March 8, 2017

To Whom It May Concern:

Mr. Andrew Peng is an official representative of the JEDEC Solid State Technology Association, which is the global leader in the development of standards for the microelectronics industry. JEDEC is working to help Chinese companies benefit by taking a leadership role in the development of open industry standards.

To facilitate this goal, JEDEC is developing plans for two new task groups in China:

- <u>IEDEC China Memory Task Group</u>: led by co-chairs Mr. Desi Rhoden (Chairman of the JC-42 Solid State Memories Committee) and Mr. Andrew Peng (Vice-Chairman of both the JC-63 Multiple Chip Package Committee and the JC-64.8 Solid State Drives Subcommittee).
- <u>JEDEC China Packaging Task Group</u>: led by co-chairs Mr. John Norton (Chairman of the JC-11 Mechanical Standardization Committee) and Mr. Andrew Peng (Vice-Chairman of both the JC-63 Multiple Chip Package Committee and the JC-64.8 Solid State Drives Subcommittee).

JEDEC looks forward to engaging with more Chinese companies and government entities in the global microelectronics standards development processes with the formation of JEDEC China Task Groups.

Sincerely yours,

Injan Que Nas

Mian Quddus Chairman

John J. Kelly

Procident

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JEDEC Solid State Technology Association, the global leader in the development of standards for the microelectronics industry, is committed to ensuring that Chinese electronic designers and manufacturers have access to timely information on the latest standards generated by JEDEC committees and have the opportunity to participate in the JEDEC standards development process.

JEDEC encourages all Chinese electronic designers and manufacturers to join the new JEDEC Task Groups, interact with JEDEC member companies and take their place with other leaders in the global microelectronics industry.

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Memory Plays a Vital Role in Building the Connected World

The Internet of Things



Source: The Register, 5 May, 2014

