2013 SEMICON China 3D-IC Forum

Commercializing TSV 3DIC Wafer Process Technology Solutions for Next Generation of Mobile Electronic Systems

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Semiconductor Manufacturing International Corporation
March 20, 2013
Safe Harbour Statement

Effective Date: 16 May, 2012

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Outline

- Driving Forces for 3DIC at System & Device Levels
- TSV-based 3DIC SiP for Handheld to Wearable
- Technology Readiness across Supply-Chain
- Outweighing Controlling Factors in Solutions & Evolution
- Collaborative Supply-Chain 3DIC Foundry Model
- Closing Remarks
Evolution in Electronic System, IC Packaging & Device

**Dominant Systems**
- IBM “ENIAC” Computer
- PC Era
- Palm
- 2G/3G MP
- Ultra-book
- Smartphone
- Tablets
- Smart-watch
- Smart-glass

**Packaging Formats**
- Discrete PKG
- DIP PKG
- TSOP
- BGA
- FC-BGA
- MAP+ POP
- FC-POP
- WLP
- 2.5DSiP
- 3DSiP
- 3DIC

**Si Devices & IC**
- 1st CPU - um
- 1st Bipolar
- 1st IC
- 1st CMOS
- Pentium 4
- 32nm CPU (HKMG)
- A6 APU
- Quantum Devices?
- MeFET?

**Timeline**
- 1950
- 1970
- 1990
- 2000
- 2010
- 2020

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### Phone-Tablet-Wearable: Core Features & Enablers

<table>
<thead>
<tr>
<th>Core Functions</th>
<th>Communication</th>
<th>Computing</th>
<th>Connectivity</th>
<th>Display &amp; interaction</th>
<th>Battery &amp; power management</th>
<th>Imaging &amp; sensing</th>
<th>Key enabling factors over all functions</th>
</tr>
</thead>
</table>
|                         | • Multi band 2.5/3G/LTE wireless FE & baseband | • ARM core APU 
  • GPU | • Bluetooth, WiFi 
  • GPS, FM | • High Res, touch sense Integrated display 
  • Controller/interface | • Thin high capacity battery 
  • PMU supporting all IC | • High Res & video CIS 
  • 10-degree motion sensing 
  • Multi noise cancelling mic | • Acceptable cost 
  • Thin format 
  • High performance (inc LP) |
|                         | • Multi band 2.5/3G/LTE wireless FE & baseband | • Multicore low power APU or LP CPU 
  • GPU | • Bluetooth, WiFi 
  • GPS, FM | • Highest Res, touch sense Integrated display 
  • Fast controller/interface | • Thin, highest capacity battery 
  • PMU supporting all IC | • High Res & video CIS 
  • 10-degree motion sensing 
  • Multi noise cancelling mic | • High performance 
  • Acceptable cost 
  • Thin format |
|                         | • Multi band 2.5/3G/LTE wireless FE & baseband | • ARM core APU 
  • GPU | • Bluetooth, WiFi 
  • GPS, FM | • Projection, bright & mini display 
  • Voice control interface | • Compact high capacity battery 
  • 1 PMU mini overall power | • Ultra compact camera 
  • 10-degree motion sensing 
  • Mini N/S cancelling mic’s | • Ultra small, thin 
  • Ultra low power 
  • Acceptable cost |
## Evolution of IC & Electronic System Integration

<table>
<thead>
<tr>
<th>Now</th>
<th>Further</th>
<th>Related Technology Enhancements</th>
<th>TSV 3DIC: Pro &amp; Con</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dominant Driving of Systems</strong></td>
<td><strong>Smartphone Tablet</strong></td>
<td><strong>e-Wearable's: Smart-watch Smart-glass</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Trend: IC &amp; Subsystem Packaging</strong></td>
<td><strong>PoP, MCM, Discrete on PCB</strong></td>
<td><strong>More “3D” SiP on PCB, less discrete &amp; isolated MCM</strong></td>
<td>++</td>
</tr>
<tr>
<td><strong>IC Devices &amp; Fabrication</strong></td>
<td><strong>HKMG to FinFET</strong></td>
<td><strong>FinFET bulk Si, SOI</strong></td>
<td>++</td>
</tr>
</tbody>
</table>

- **Pro**: Better device variation management
- **Con**: Decouple logic with MS/RF to 2 chips, maybe at different nodes or technologies

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### Example: Chips to SiP Grouping on Smartphone PCB

<table>
<thead>
<tr>
<th>Front Side</th>
<th>MCP/SiP</th>
<th>TSV SiP Opt</th>
<th>Back Side</th>
<th>MCP/SiP</th>
<th>TSV Opt</th>
</tr>
</thead>
<tbody>
<tr>
<td>WiFi module</td>
<td>WiFi Combo wireless processor WIFI FE</td>
<td>May use TSV SiP but costly</td>
<td>APU</td>
<td>DRAM MCP</td>
<td>TSV Wide I/O best option but costly &amp; manufacturability</td>
</tr>
<tr>
<td>3-axis gyro</td>
<td>MEMS+ASIC SiP</td>
<td>TSV SiP: thinner, better noise isolation</td>
<td>LTE Baseband Processor</td>
<td>PMIC on front-side connected through PCB</td>
<td>Split logic potion with MS/RF to two chips, 2.5D SiP</td>
</tr>
<tr>
<td>3-axis accelerometer</td>
<td>MEMS+ASIC SiP</td>
<td>Combo SiP: Single chip</td>
<td>Audio Chips</td>
<td>1/2 Chip MCP</td>
<td>May stay separated for noise isolation</td>
</tr>
<tr>
<td>Touch screen controller</td>
<td>BCM interface</td>
<td>Performance gain but costly</td>
<td>Imaging Sensor Camera Module</td>
<td>8 or 13M BSI</td>
<td>Can further thinner WL camera module</td>
</tr>
<tr>
<td>GSM/GPRS/EDGE PA</td>
<td></td>
<td></td>
<td>Microphones</td>
<td>3 in different packages &amp; sites</td>
<td>No help</td>
</tr>
<tr>
<td>CDMA PA</td>
<td>SiP with matching switches, IPD, LNA</td>
<td>TSV SiP for PA module: improving noise performance, but cost needs justification</td>
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<tr>
<td>GSM PA</td>
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<td>LTE PA</td>
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<td>Multiband FE</td>
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<td>WCDMA PA</td>
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</table>
Device Level: Alternative “Process Integration”

- Dedicated memory MOS
  - Better fine pitch dense array & OPC
  - Optimized implants & thermal budget

- Dedicated specialty MOS
  - Gross litho CD & variable patterns
  - Specialized implants & analog tuning

- Enhanced, dedicated CMOS (FinFET) design
  - Better ultra fine CD & OPC control
  - Simplified baseline implants & thermal budget

- HS/LP dominant (to FinFET)
  - Ultra fine CD, fine array
  - Baseline implants & constrained thermal budget

- 2 Poly Cell
  - Fine pitch stacked array
  - Special implants & thermal budget

- Specialty MOS
  - Large CD range & patterns
  - Special implants & analog performance

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1. FEOL CD => ~10nm, BEOL CD ~10’s nm; narrowing long on-chip interconnects
2. IMD advance (LK => ELK) cease & limit further RC reduction
## Readiness in Supply Chain for Manufacturability

<table>
<thead>
<tr>
<th>Via-Mid Front-end</th>
<th>TSV-mid litho</th>
<th>TSV-mid etching</th>
<th>TSV-mid isolation</th>
<th>Barrier/seed DEP</th>
<th>TSV ECP</th>
<th>Post ECP Cu CMP</th>
<th>BEOL/FS-RDL/Bump</th>
</tr>
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<tbody>
<tr>
<td>Foundry process</td>
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<td>Capability vs. spec</td>
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<td>Process Window &amp; Uniformity</td>
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<td>Tool maturity</td>
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<tr>
<td>Running cost &amp; throughput</td>
<td>Acceptable for risk run</td>
<td>Ready for pilot</td>
<td>Mature 4 mass production</td>
<td>Close to acceptable</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Via-Mid Middle-end</th>
<th>Stacking &amp; Bonding</th>
<th>Temp bond to carrier</th>
<th>Thinning /grinding</th>
<th>TSV reveal</th>
<th>Carrier debonding</th>
<th>Inspect &amp; metrology</th>
<th>WL &amp; SiP Testing</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSAT Process</td>
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<td>CtC</td>
<td>CtW</td>
<td>WtW</td>
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<td>Capability vs. spec</td>
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<td>Window, Unif’ty</td>
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<td>Tool maturity</td>
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<tr>
<td>Running cost &amp; throughput</td>
<td>Not ready</td>
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## TSV 3DIC Implementation Roadmap: Pro & Con

<table>
<thead>
<tr>
<th>Key Pro Factors</th>
<th>Key Con Factors</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Data speed</td>
<td>• KGD</td>
</tr>
<tr>
<td>• PKG thickness</td>
<td>• Cost</td>
</tr>
<tr>
<td>• Yield</td>
<td>• Technical feasibility</td>
</tr>
<tr>
<td>• Speed</td>
<td>• TSV-CMOS</td>
</tr>
<tr>
<td>• PKG thickness</td>
<td>• I/O interface</td>
</tr>
<tr>
<td>• Wafer process</td>
<td>• Cost (unless performance justified)</td>
</tr>
<tr>
<td>• Noise isolation</td>
<td>• Difficult for large format chips</td>
</tr>
<tr>
<td>• PKG thickness</td>
<td>• Cost reduction thru WLP</td>
</tr>
<tr>
<td>• Noise isolation</td>
<td>• Functional requirements</td>
</tr>
<tr>
<td>• Cost reduction thru WLP</td>
<td>• Cost reduction thru WLP</td>
</tr>
<tr>
<td>• Technical feasibility</td>
<td>• Difficult for large format chips</td>
</tr>
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3DIC Commercialization: Key Paradigm Factors

Research & Pathfinding domain

Boosting Performance
- Speed/bandwidth
- Power reduction

Development & improvement domain

Reducing Form Factor
- Thinner
- Smaller

Better Manuf’bility
- Overall cost
- Supply chain readiness

Existing technology: PoP SiP on substrate

Competing technology: Thru-Glass Interposer To TSV 2.5D Interposer

Commer-Cialization domain

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Emerging Mid-End & Two Ecosystem Models

- Technical spec (DR, etc) & hand-off: must shared from FE, ME, BE to system
- Productization & commercialization only verified along full line down to system level
- Foundry & OSAT best to leverage existing differentiating but matching core strength & capability over ME, extended from FE and BE respectively

"VERTICALLY INTEGRATED" wafer + package manufacturing foundries

"COLLABORATIVE" supply-chains between wafer foundries & packaging subcontractors

"VIRTUAL IDM" new ecosystems

Courtesy of Yole
Collaborative Full 3DIC Foundry Services

<table>
<thead>
<tr>
<th>Key Competency &amp; Services</th>
<th>IC Design</th>
<th>Devices on Wafer Fab &amp; WL Testing</th>
<th>Wafer Level Packaging</th>
<th>Chip to System Packaging &amp; Testing</th>
<th>System &amp; Board Assembly</th>
<th>(Sub) System Design &amp; Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDM’s Or wafer + WLP + P&amp;T</td>
<td>Complete vertical integration</td>
<td>Full foundry model</td>
<td>Ext Service Or sub con</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fab-lite &amp; fabless</td>
<td>Core Value &amp; Strength</td>
<td>Extended engineering design for sub con</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>CMOS Wafer Foundry</td>
<td>Design Service</td>
<td>Core Value &amp; Strength</td>
<td>TSV Via-mid</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WLP Partner</td>
<td>Ext Serv</td>
<td>Core Value &amp; Strength</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Chip &amp; SiP &amp; Testing Partner</td>
<td>Collaborative 3DIC Foundry Model</td>
<td>Expanded service</td>
<td>Core Value &amp; Strength</td>
<td>Ext Service</td>
<td></td>
<td></td>
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<tr>
<td>System Assembler &amp; User</td>
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Closing Remarks

Systems towards mobile wearable fundament to driving supply chain to TSV 3DIC development & commercialization

• Mobile, handheld to wearable inevitable, the dominant trend
• Main electronic boards forced to shrink in size and thickness
• Core & peripheral chips continue to regroup to smaller, thinner SiP; isolated functional chips thinner, smaller; discrete devices to consolidate into SiP or SoC

Miniaturization, performance boost and overall manufacturing cost: tri-driving and limiting factors in paradigm of commercialization

• Scenario 1: performance gain outweighing increase in overall cost
• Scenario 2: 3D WLP and miniaturization also reducing overall cost
• Scenario 3: ultra thin becoming must for system & SiP integration

Collaborative TSV 3DIC foundry service: adequate model to address overall supply chain manufacturability & costs

• Leverage available R&D resources of accumulated expertise, manufacturing lines, minimize overall capital investment and running costs
• Sustain & growth supply-chain ecosystem in collaborative evolution
Thank You
Semiconductor Manufacturing International Corporation
SMIC
Q&A
谢谢各位