中国最大的面向半导体产业的国际技术研讨会

2011年中国国际半导体技术大会（CSTIC）将于3月13－14日在上海与SEMICON China同期举办，这是中国规模最大、技术水平最高的面向半导体产业的年度盛会，内容不仅涉及半导体器件、材料与工艺，而且涵盖前沿半导体技术及硅材料技术与应用。

大会由两大国际行业协会SEMI、ECS（电化学协会）及中国高科技专家委员会共同主办，研讨会旨在为半导体与光伏产业技术人员及科研人员提供国际水平的交流平台，以促进海内外业界人士、客户与同行的沟通、提高中国技术水平为目的。研讨会同时也是半导体相关企业拓展中国与亚洲市场的良好机会。

目前大会已收到业界投稿390篇，超过100名全球知名半导体、光伏与LED技术专家将为大会带来特邀精彩报告。

主办方：国际半导体设备及材料协会（SEMI）
美国电化学协会（ECS）
中国电子商会（CECC）

共同主办方：中国国家高科技专家组（CHTEC）

协办方：国际电气和电子工程师协会（IEEE）
国际材料研究协会（MRS）
中国电子材料行业协会（CEMIA）
中国化学学会电化学分会（CSE）
Plenary Session

**Dr. David Wang**
President & CEO
SMIC, China

**Dr. Tze-chiang Chen**
IBM Fellow, USA

**Dr. Chenming Hu**
TSMC Distinguished Chair Professor of Microelectronics, UC Berkeley, USA

**Dr. John H. Lau**
ITRI Fellow, Industrial Technology Research Institute, Taiwan, China

Symposium I. Design and Device Engineering

* Zhbin Ren
  IBM
  Leakage engineering enabling PDSOI Ring Oscillators operating in sub-100pA/um Ioff regime

* Frank Bin Yang
  Globalfoundries
  Advanced Strain Techniques for state-of-the-art CMOS

* Qing Liu
  ST Micro Electronics
  Double Gate ETSOI devices

* J.J.Liou
  University of Central Florida
  Electrostatic discharge (ESD) challenges in nanowire technology

* Chenshin Lien
  Tsinghua University
  High Performance HIO, Based Resistive with Sub-Nanosecond Switching Speed and Excellent Endurance

* Qingtai Zhao
  Forschungszentrum Julich, Germany
  Advanced nano-scaled CMOS devices

* Zhengqiang Ma
  Wisconsin University
  Fast Flexible Electronics Based on Printable Thin Mono-Crystalline Silicon

* Danny Shum
  Infineon
  Advanced memory technology

* Li Mingfu
  Fudan University
  A dialogue with CMOS Industry — How inappropriate test scheme misguides your product reliability

* Tenko Yamashita
  IBM
  Opportunities and challenges of FinFET device as a candidate for 14nm node CMOS Technology

* Brian Chen
  acetelicon
  ETSOI Modeling with BSIMSOI

* W.C. Chien
  Macronix
  Advanced RRAM technology

Symposium II. Photolithography and Patterning

* Andreas Erdmann
  Fraunhofer IISB
  Compensation of mask induced aberration effects

* Benjamin Szu-Min Lin
  Cymser Southeast Asia Ltd.
  Cymer LPP EUV source system development status

* Qiang Wu, Verne Xu, Michael Hao, Winnie Liu, Xuelong Shi and Yiming Gu
  SMIC
  Limit of Line End Shortening Correction under Single Exposure in 193 nm Immersion Lithography

* Yiming Gu, Xuelong Shi, Qiang Wu, and Alien Lin
  SMIC
  Immersion Lithography in China

* Kurt Ronse
  IMEC
  Lithography options for 22nm and beyond

* Lee Pang
  Luminescent

* Tony Yen
  TSMC

* Vivek Singh
  Intel

* Soichi Irie
  Toshiba

* Gregg Gallatin
  NIST

* Yoshihiro Yamamoto
  Dow Chemical

* Chang Zhou
  SMIC
  300mm Wafer Stepper for Advanced package application

Symposium III. Dry & Wet Etch and Cleaning

**Olivier Joubert**
CNRS LTM, France
Plasma Etching Challenges involved in Gate Stack Patterning for 45 nm technological nodes and below

* Cathy Labelle
  Globalfoundries
  Plasma Etching Challenges in BEOL for 45 nm nodes and beyond

* Sebastian Engelmann
  IBM Research
  Plasma etching of advanced gate stacks

* Seiji Samukawa
  Tohoku University
  Ultimate Top-down Processes for Future Nanoscale Devices

Symposium IV. Thin Film Technology

* Adelmann, Christoph
  IMEC, Belgium
  Rare earth aluminate thin films for non-volatile memory applications

* Afanasiev, Valeri
  KU Leuven, Belgium
  Electronic states at interfaces of metal, semiconductors, and insulator

* Baklanov, Mikhail
  IMEC, Belgium
  Challenges of scaling of ultra low-k dielectric materials

* Jourdan, Nicolas
  IMEC, Belgium
  PVD RuTa process screening for advanced interconnects application

* Kim, Hyungjun
  Yonsei University, Korea
  Atomic layer deposition for nanoscale semiconductor devices

* Kuppurao, Satheesh
  Applied Materials, USA
  Thin Film Processes for 3D SiGe and SiC

* Lin, Wan-Yu
  KU Leuven, Belgium
  Low cost solution-processed high-k gate dielectric materials for large area applications

* Schaeckers, Marc
  IMEC, Belgium
  ALD Ru and its application in MM cap and BEOL

* Subramonium, Pramod
  Novellus, USA
  PECVD Applications for 32 nm Node and Beyond

* Yeo, Yee-Chia
  National University of Singapore
  Technology options for reducing contact resistances in sub-22 nm transistors

* Zhang, Wenhui
  IMEC, Belgium
  Fine pitch micro-bump interconnections for advanced 3D chip stacking

* Zhao, Chao
  Institute of Microelectronics, China
  Gap fill processes for high AR structures

* Rachmady, Willy
  Intel, USA
  Non-Silicon high-mobility channel materials for future high speed and low power logic transistors
Symposium V.CMP and Post-CMP Cleaning

* Shumin Wang  
  Anji Microelectronics
* James LaCasse  
  NexPlanar Corporation
* Youngsik Moon  
  Global Foundries
* SY Yoon  
  Ehwa
* S. V. Babu  
  Clarkson University
* Yohei Yamada  
  Hitachi
* Cliff Spiro  
  Cabot Microelectronics
* Rakesh Singh  
  Entris
* Hitoshi Morinaga  
  FUJIMI
* Rita Vos  
  IMEC
* Gautam Banerjee  
  Air Products
* Katia Devriendt  
  IMEC
* Rob Rhoades  
  Entropix
* Srinivasa Raghavan  
  UA

Symposium VI. Materials and Process Integration for Device and Interconnection

** Chia-Hong Jan  
  Intel
* Yasushi Akasaka  
  TEL
* Schram, Tom  
  IMEC, Belgium
* Yu, Hong Yu  
  Nanyang Technology University, Singapore
* Chung Lam  
  IBM Watson Research center
* Jing Li  
  IBM Watson Research center
* Satya V. Nitta  
  IBM Watson Research center

Symposium VII. Packaging and Assembly

** Dongkai Shangguan  
  Technology & Engineering and Senior Fellow Rextronics International
* Herb Huang  
  SEMIC
* Hiroki Suzuki  
  Electronic Device Materials Research Laboratory II (EDL2), Information and Telecommunication Material Laboratories (ITML), Sumitomo Bakelite Co., Ltd.
** Calvin Cheung  
  VP of Engineering at ASE(US)
** Leo Linehan  
  Dow Electronic Materials
* Lei Shi  
  Nantong Fujitsu
* Young-Ho Kim  
  Hanyang University
** Young-Do Kweon  
  Samsung Electro-Mechanics Co. Packaging Requirements for Next Generation Mobile Application

Symposium VIII. Metrology, Reliability and Testing

** Robert Aitken  
  ARM, USA
* Larry Zhao  
  IMEC, Belgium
* Ting-Pu Tai  
  Mentor Graphics
* Kenji Sakurai  
  University of Tsukuba, Japan
* Wenbing Yun  
  Xradia, US
* Carole Graas  
  IBM
* Brain Ji  
  SUNY-Albany
* Jinghong (John) Li  
  IBM

Symposium IX - Emerging Semiconductor Technologies

** Kai Cheng  
  IMEC
* Guy Brammertz  
  IMEC
* Do Young Kim  
  Yonsei University, Korea
* Gill Lee  
  Applied Materials, Korea
* Aimin Song  
  University of Manchester
* Michael Fritze  
  University of Southern California
* Chunming Niu  
  University of Tokyo
* Padma Gopalan  
  University of Wisconsin-Madison
* Grant Willson  
  University of Texas at Austin
* Takayuki Ohba  
  University of Tokyo
* Dennis Lin  
  IMEC

Symposium X - Silicon Materials for Electronic and Photovoltaic Applications

** Tore Torvund  
  REC Silicon
* Rommel Noufi  
  NREL, USA
* Jeff Yang  
  Uni-solar Ovonic
** Y. Ohshita  
  Toyota Institute of Technology
* M. Tajima  
  JAXA
* Sekiguchi  
  NIMS
* Michael Seibt  
  Goettingen University, Germany
* Xuegong Yu  
  Zhejiang University
* Euisong Shin  
  Yonsei University, Korea
** Kenji Sakurai  
  Xradia, US
** Renhe Jia  
  Applied Materials, USA
* Dan Martin  
  SEMI

** Hikavyy, Andriy  
  IMEC, Belgium
  Selective epitaxial growth: trends in a modern p-MOS transistor device integration
* Shi, Xiaoping  
  IMEC, Belgium
  Review of Silicon nanowire Oxidation
** Moinpour, Mansour  
  Intel, USA

Symposium VIII. Metrology, Reliability and Testing

** Robert Aitken  
  ARM, USA
* Larry Zhao  
  IMEC, Belgium
  Key interconnect reliability challenges for 22nm and beyond
* Ting-Pu Tai  
  Mentor Graphics
  Test and diagnostics
** Kenji Sakurai  
  University of Tsukuba, Japan
  Metrology
* Wenbing Yun  
  Xradia, US
  Metrology
** Carole Graas  
  IBM
  Reliability
* Brain Ji  
  SUNY-Albany
  Test and Characterization
* Jinghong (John) Li  
  IBM
  Channel Strain Characterization and Measurement in Semiconductor Devices

Symposium IX - Emerging Semiconductor Technologies

** Kai Cheng  
  IMEC
  Gain-on-Si blue LED and Power Switching Devices
* Guy Brammertz  
  IMEC
  Electrical quality of III-V/oxide interfaces: good enough for MOSFET devices?
* Do Young Kim  
  Yonsei University, Korea
  Transparent electronics and photovoltaics
* Gill Lee  
  Applied Materials, Korea
  Emerging process technology
* Aimin Song  
  University of Manchester
  Single-layered planar nanodevices for THz imaging and energy harvesting
* Michael Fritze  
  University of Southern California
* Chunming Niu  
  University of Tokyo
* Padma Gopalan  
  University of Wisconsin-Madison
* Grant Willson  
  University of Texas at Austin
* Takayuki Ohba  
  University of Tokyo
* Dennis Lin  
  IMEC
  Electrical characterization of the MOS (Metal-oxide-semiconductor) system: High mobility substrates

Symposium X - Silicon Materials for Electronic and Photovoltaic Applications

** Tore Torvund  
  REC Silicon
  Granular Polysilicon in Solar Industry
* Rommel Noufi  
  NREL, USA
  High efficiency CIS film solar cell technology
* Jeff Yang  
  Uni-solar Ovonic
  Thin film Si solar cell technology
** Y. Ohshita  
  Toyota Institute of Technology
  Silicon solar cells & III-N solar cells, Associate professor
* M. Tajima  
  JAXA
  PL Characterization
* Sekiguchi  
  NIMS
  CL Characterization
* Michael Seibt  
  Goettingen University, Germany
  Defect control in crystal silicon
* Xuegong Yu  
  Zhejiang University
  Silicon water cleaning
* Euisong Shin  
  Yonsei University, Korea
  Thin film technology review for solar cell
** Kenji Sakurai  
  Xradia, US
** Renhe Jia  
  Applied Materials, USA
* Dan Martin  
  SEMI
  Silicon Market Analysis

* Hikavyy, Andriy  
  IMEC, Belgium
  Selective epitaxial growth: trends in a modern p-MOS transistor device integration
* Shi, Xiaoping  
  IMEC, Belgium
  Review of Silicon nanowire Oxidation
** Moinpour, Mansour  
  Intel, USA
会议主席

Dr. Hanming Wu
SMIC

会议技术专家委员会

Dr. Qinghuang Lin
Executive Co-Chair
Symp. IX Chair
IBM, USA

Dr. Ying Zhang
Symposium III Chair
IBM, USA

Dr. Cor Claeys
Conference Co-Chair
IMEC, Belgium

Dr. Jiongping Lu
Symposium IV Chair
SMIC, China

Dr. David Huang
Conference Co-chair
Symposium X Chair
Praxair Inc., USA

Dr. Ara Philipossian
Symposium V Chair
University of Arizona, USA

Dr. Yue Kuo
SESEA Award Chair
Texas A&M University, USA

Dr. Ran Liu
Symposium VI Chair
Fudan University, China

Dr. Ru Huang
Symposium I, Chair
Peking University, China

Dr. Tom Jiang
Symposium VII Chair
Maxim Integrated Products Inc. USA

Dr. Kafai Lai
Symposium II Chair
IBM, USA

Dr. Peilin Song
Symposium VIII Chair
IBM, USA

http://semiconchina.semi.org/cstic
中国国际半导体技术大会
China Semiconductor Technology International Conference

2010年3月13－14日
上海浦东嘉里大酒店

会议指导委员会
Roque Calvo ECS Representative
Allen Lu SEMI China
Hiroshi Iwai Tokyo Institute of Technology, Japan
Tomi T. Li National Taiwan Central University

会议顾问委员会
Minhwa Chi SMIC, China
Philip Wong Stanford University
Swami Mathad Tech Consulting, USA
Hsing-Huang Tseng Texas State University
Steve Yang GSMC, China
Qingyuan Han Hans Consulting International, USA
Shichang Zou Chinese Academy of Sciences, China
Hailing Tu GRINM, China

会议委员会
Symposium I
Shaoning Mei HHNEC, China
Huilong Zhu IME, China
Boyong He CSMC, China
Huiling Shang IBM, USA
Hong Wu SMIC, China
Frank Bin Yang Globalfoundries, USA

Yiming Gu SMIC, China
Xiaoming Ma Dow Chemical
Zewen Liu Tsinghua University, China
Benjamin Lin Cyner, Taiwan
Linyong (Leo) Pang Luminescent, USA
Da Yang Chinese Academy of Science

Symposium II
Tom Ni AMEC, China
Jinrong Zhao Microelectronics, China
Maxime Darnon French institute for scientific research
Sebastian Engelmann IBM, USA
Masahiro Sumiya Hitachi High-Technologies, Japan
Denis Shamiryan IMEC

WeiE Wang Intel, Belgium
Zhen Guo Intel, USA
Jason Tian Nikon Precision, China
Canyuan Wang Tokyo Electron, China
Jin Reid Novellus, USA
YuLong Jiang Fudan University, China
Xiaoping Shi IMEC, Belgium
Duofeng Yue TI, USA
Kyoichi Suguro Memec Toshiba, Japan

Symposium III
Shumin Wang Anji Microelectronics, China
Charles Xing SMIC, China
Jingxun Fang HHNEC, China
Kailiang Zhang Tanjin University of Science & Technology, China
KuoChun Wu Cabot Microelectronics, Asia
Mahadevaiyer Krishnan IBM, US

Gary Ding Intel, US
Weichung Yu Dow Chemical
Paul-Chang Lin SMIC China
Takenao Nemoto Tohoku University, Japan
Yohei Yamada Hitachi

Symposium VI
Frank Chen SMIC, China
Sownyna Krishnan SEMITRAC, USA
Massayasu Tanjyo Nissin Ion Equipment
Ganming Zhao Applied Materials
Zheyao Wang Tsinghua University, China
Archie Liao Air Products, China
Da Zang Freescale
Larry Zhao Intel

Symposium VII
Lixi Wan Institute of Microelectronics, China
Daniel Lu Henkel China
Jason Shi K&ES, China
Ricky S W Lee Hong Kong University of Science and Technology, China
Roy Yu IBM, USA
Yishao Lai ASE, Taiwan, China
Young Do Kweon Samsung, Korea
Jing Shi Oracle, USA
Herb Huang SMIC, China

Symposium VIII
Bin Wang Spansion, China
Wen-li Wu NIST, USA
Yuhua Cheng Peking University, China
Francis Jen KLA-Tencor, China
Kelvin Xia Verigy, China
Srinivas Raghvendra Synopsys
Xiaowei Li Institute of Computing Technology, Chinese Academy of Sciences
Yu Huang Mentor Graphics, USA
Qiang Guo SMIC, China
Jian-fu Zhang Liverpool John Moores University

Symposium IX
Jia Chen IBM, USA
Edward Y. Chang National Chiao Tung University, China
Jing Kong MIT, USA
Hyungjun Kim Yonsei University
Jinn P. Chu National Taiwan University of Science and Technology, China
Jie Zhang Singapore
Fuhua Yang Institute of Semiconductor, Chinese Academy of Sciences, China
Wang Yueh Intel, USA
Paul R. Berger Ohio State University, USA

Symposium X
Koichi Kakimoto Kyushu University, Japan
DerenYang Zhejiang University, China
Henry Erk MEMC, USA
Jenq-yang Chang National Central University, Taiwan, China
Qi Wang NREL, USA
Renhe Jia Applied Materials, USA
Timmy Bao BTU International, USA
Symposium I: Design and Device Engineering

Session I: Advanced Memory Technology
Session chairs: Ru Huang
13:15-13:20
Chairman Remarks
13:20-13:45
**Embedded Non-Volatile Memories
Danny Shum, Infineon
13:45-14:10
*High Performance HfOx Based Resistive Memory with Sub-Nanoscale Switching Speed and Excellent Endurance
1. Tsing Hua University; 2. Industrial Technology Research Institute; 3. Minghsin University of Science & Technology, Taiwan, China
14:10-14:35
*Recent Progress on WOx-based and Cu-based Resistive Switching Memories (ReRAMs)
Mackrom International Co., Ltd.
14:35-15:00
A Novel High Programming Efficiency and Highly Scalable Flash Memory Cell Based on TFET
Shiqiang Qin, Poren Tang, Yimao Cai, Qianqian Huang, Yu Tang, Ru Huang
Peking University
15:00-15:05
Stacked high-k Charge Trapping Layer for High Performance Flash Memory Application
Zhiwei Zheng, Zongliang Huo, Manhong Zhang, Qin Wang, Chenxin Zhu, Jing Liu, Ming Liu
Institute of Microelectronics of Chinese Academy of Sciences
15:05-15:20
A Novel Floating-Junction-Gate DRAM Utilizing Gated-diode
Song-Bin Zhang, Xie Lin, Lei Liu, Xin-Yan Liu, Cheng-Wei Cao, Pong-Fei Wang, DaWei Zhang
1. School of Microelectronics, Fudan University; 2. Oriental Semiconductor Co., Ltd., Suzhou, China
15:20-15:35
Deposition of ZnO Films by Sputtering and Its Resistive Switching Properties
Wang Fang, Yang Baohe, Wang Lanlan, Song Kai, Zhang Kailiang
1. Tianjin University of Technology; 2. Tianjin University
15:35-15:50
Coffee Break

Session II: SOI Device and Advanced Process Technology
Session chairs: Cor Claeyes
15:50-16:15
*Leakage Engineering Enabling PDSOI Ring Oscillators Operating in sub-100pA/µm Ioff Regime
Zhibin Ren, IBM
16:15-16:40
*Ultra-thin Body and BOX (UTBB) Device for Aggressive Scaling of CMOS Technology
1. STMicroelectronics; 2. Toshiba; 3. IBM; 4. Renesas; 5. CEA-LETI; 6. Globefoundries
16:40-17:05
*Assessment of Extremely Thin SOI MOSFET Modeling with BSIMSOI
Brian Chen, Accelicon Technologies, Inc.
17:05-17:20
Simulations of FDSOI CMOS with Asymmetric Back Gate
Miao Xu, Chengjing Liang, Huifeng Zhu, Haishu Yin, Zhijong Luo
Institute of Microelectronics of Chinese Academy of Sciences
17:20-17:35
ILD0 CMP Process Development for 32nm Gate Last Approach
Qun Shao, Chengjing Wang, Kui Li, Peng Chen
Semiconductor Manufacturing International Corporation
17:35-17:50
Scaling MOSFETs with Self-aligned Super-Steep-Retrograded Halo (SSRH)
Binneng Wu, Weiping Xiao, Huifeng Zhu, Chengjing Liang, Hao Wu, Haishu Yin, Zhijong Luo, Hongyu Yu
Institute of Microelectronics of Chinese Academy of Sciences

Session III: Characterization, ESD and Reliability
Session chairs: Boyong He
8:30-8:55
**Electrostatic Discharge (ESD) Challenges in Silicon Nanowire Technology
J.J. Liou, University of Central Florida
8:55-9:20
*A Dialogue with CMOS Industry - How Inappropriate Test Scheme Misguides Your Product Reliability
Li Mingfu, Fudan University
9:20-9:35
Characterization of Random Telegraph Signal Effects for 0.18um Technology
Yuanqian Ji, Sutter Dai, Minxia Wei, Sunny Zhang, Daniel Xu
Grace Semiconductor Manufacturing Corporation
9:35-9:50
The Effect of AlGaN Barrier Thickness on the Noise of AlGaN/GaN High Electron Mobility Transistors
R. Yahyazadeh, Z. Hashempour, M.A. Eskandarzadeh
Islamic Azad University - Khoy branch

Schedule as of Jan 19. Agenda is subject to change. Visit http://semiconchina.semi.org/cstic for current information.
09:00-10:05
Extraction and Analysis of Substrate Parameters in On-Chip Spiral Inductor Model
Xi Li', Zheng Ren', Dawei Chen', Yanling Shi'
1. East China Normal University, China;
2. Shanghai Integrated Circuits Research & Development Center
10:05-10:20 Coffee Break

Session IV: Nano CMOS Devices and Process Technology
Session chairs: Shaoning Mei
10:20-10:45 *Opportunities and challenges of FinFET device as a candidate for 14nm node CMOS Technology
Teru Nakagami, IBM
10:45-11:00 Structural Effects of Channel Cross-section on a Gate Capacitance of Silicon Nanowire Field-effect Transistors
Shiho Sato1, Kusukuri Kakushina1, Pathal Alme1, Kenji Chinn2, Kenji Naito2, Keisaku Yamada1, Hiroshi Iwai1
11:00-11:15 Process Impact and Design Optimization on the Soft Yield of 25nm FinFET SRAM Cells
Meng Li, Qingqing Liang, Huifeng Zhu, Huicai Zhong
Institute of Microelectronics of Chinese Academy of Sciences
11:15-11:30 TiN/W/LaO/Si High-k Gate Stack for EOT below 0.5nm
P. Atme1, D. Kitayama1, T. Kanie1, T. Suzuki1, T. Koyanagi1, M. Kizuki1, M. Mamatafisal1, T. Kawai1, K. Kakushina1, K. Tsutsumi1, A. Matsumiya1, N. Sugiy1, K. Naito1, T. Hatton1, H. Iwai1
1. Frontier Research Center, 2. Tokyo Institute of Technology
11:30-11:45 PMOS Source/Drain Extension Implantation Species Impact on Device and SRAM Performance
Jinhua Liu1, Weihao Fu2, Lina Zhang3
Institute of Microelectronics of Chinese Academy of Sciences
11:45-12:00 Hollow FinFETs (hFinFETs): A 3D Simulation Study
Weiping Xiao1, Hao Wu2, Huiling Zhu3, Qingqing Liang3, Zhiling Luo3, Haichao Yin
Institute of Microelectronics of Chinese Academy of Sciences
12:00-13:15 Lunch

Session V: Novel Device and Process Technology
Session chairs: Huilong Zhu
13:15-13:40 *Silicon and Strained Silicon Planar and Nanowire Tunnel FETs
C. Sandow, S. Schmidt, S. Richter, W. Yu, B. Zhang, Q. T. Zhao and S. Mantl
Forschungszentrum Julich, Germany
13:40-13:55 Short Gate Tunnel-FETs for Low Voltage Digital Applications
Jing Zhuge1,2, Anne S. Verhulst1, Willem G. Vanderbergh1, Wilm Dehaene1,2, Ru Huang1, Yanguang Wang1, Guido Groeseneken1
1. IMEC, 2. Peking University, 3. K. U. Leuven
13:55-14:10 A Novel Tunnel Oxide Based Tunnel FET
Heli Wang, Zhiling Luo, Haichao Yin, Huiling Zhu, Jia Lu, Zhengyong Zhu
Institute of Microelectronics of Chinese Academy of Sciences
14:10-14:25 STI CMP: Exploration of a Silica Based Slurry System
Peter Song1, Daisy Yao2, Jack Dawsun3
1. Anji Microelectronics (Shanghai) Co., Ltd.
14:25-14:40 Linearity Improvement on MIM Capacitors
Chu T.P., Yang P., Evie Kho, Ang Y.K., Tia S.H.
14:40-14:55 Double Hump Effect Suppression in High Voltage LDNMOS
Haiying Ling, Steve Yang, Kevin Huang, Zijing Ye, Xifeng Gao, Liang Zhao
Grace Semiconductor Manufacturing Corporation
14:55-15:10 Modeling of Electron Transport in III-Nitride Compound Semiconductors for Low Field and Low Temperature Applications
Souad M. Elshahawi1, Seryamreee Gupta1, Somnath Chatterjee1, T. K. Chakraborti
Techno India, Salt Lake, Kolkata, India
15:10-15:25 Coffee Break

Session VI: Flexible Technology and High Voltage/Memory Devices
Session chairs: Hong Wu
15:25-15:50 *TBD
Zhenqiang Ma
Wisconsin University
15:50-16:05 MOS device for High Voltage Operation
XH Ju
Grace Semiconductor Manufacturing Corporation
16:05-16:20 HNNEC 0.18um BCD Technology for high density power integration
Zhang Shuai, Mei Shaoqing, Qian Wanzheng, Dong Ke
HNNEC
16:20-16:35 Performance Improvement of Si-NC Memory Device by Using a Novel Programming Scheme
Dandan Jiang1, Zhenqiang Lu1, Hanyun Zhang1, Jin Wang1, Xiaoman Yang1, Yong Wang1, Bo Zhang1, Junning Chen1, Ming Liu1
1. Institute of Microelectronics, Chinese Academy of Sciences; 2. Anhui University; 3. Grace Semiconductor Manufacturing Corporation
16:35-16:50 A Novel Dual Floating Gate Flash Cell Using Single Poly Processes
Xi Lin1, Lei Li1, Xin-Yan Li1, Dongke Cao1, Cheng-Wai Cao1, Peng-Fei Wang1, David Wei Zhang1
1. Fudan University; 2. Oriental Semiconductor Co., Ltd
16:50-17:05 Anomalous Behaviors of Cubic GaInN Ternary Alloys
Naci Tl1
17:05-17:20 0.18um Scalable 7~45V pLDMOS for Smart Power Application
Zhengchao Liu1, Shushu Tang1, Frank Lei1, James Shen1, Steve Yang1
1. Grace Semiconductor Manufacturing Corporation
17:20-17:35 0.18 micron BiCMOS Process with Novel Structure SiGeC HBT
Donghua Liu1, Wensi He1, Xiong Bin Chen1, Pan Chen1, Jun Hu1, Sheng An Xiao1, Xuncheng Wang1, Mei Shao1, Yu Shi1
Shanghai HNNEC Electronics Company
Symposium II: Patterning and Photolithography

Symposium Chairs:
Kafai Lai
IBM, USA
Yiming Gu
SMIC
Xiaoming Ma
Sr. Technical Sales Manager, Dow Chemical
Zewen Liu
Professor, Tsinghua University, Nano-processing Technology, China
Heping Wang
Manager, Brewer Science
Benjamin Lin
Director, Cymer, Taiwan
Linyong (Leo) Pang
Sr. VP & GM, Luminescent, USA

Session I: Keynotes

Sunday, March 13

13:15-13:20
Chairman Remarks

13:20-13:50
**EUV Lithography for Manufacturing of Logic Devices at 20 nm and Beyond
Tony Yen
TSMC

13:50-14:20
**Lithography options for 22nm and beyond
Geert Vandenberghe, Kurt Ronse
IMEC

14:20-14:50
**Immersion Lithography in China
Yiming Gu, Xuelong Shi, Qiang Wu, Alien Lin
SMIC

14:50-15:05
Coffee Break

Session II: Strategic Lithography

15:05-15:25
*Evolutionary Paths for Future Lithography beyond 20nm
Donis Flagello
Nikon Precision US

15:25-15:45
*Ultimate Optical Extension Technologies for Ultra Low-k1 Lithography Generations
Soichi Inoue
Toshiba

15:45-16:05
*Compensation of Mask Induced Aberration Effects
A. Erdmann, P. Everschizby, F. Shao, T. Fühner
Fraunhofer Inst. of Technology

16:05-16:25
*Photomask Technology for 20nm and Beyond
Yoji Tono-Oka
Toppan

16:25-16:45
*Intersecting Challenges: Computational Lithography and Computational Defect Management – The Latest Progress
Leo Pang
Luminescent

Session III: Computational Litho

Monday, March 14

8:40-9:00
*Topic in Computational Lithography
Kafai Lai
IBM

9:00-9:20
*Lithography-Driven Design Rule Definition and Optimization
Xuelong Shi
SMIC

9:20-9:40
*Photomask Optimization Using Level-set Method in Pixel Based Inverse Lithography Technology
Jinyu Zhang, Yao Peng, Yan Wang, Zhiping Yu
Tsinghua University

9:40-10:00
Full Field CDU and Overlay Characterization Model
Anatoly Burov
SMEE

10:00-10:40
A Fast OPC Algorithm for IC Layout Based on 1-D Cells after Optimized Gap Distribution
Lin Bin
Zhejiang University

10:20-10:35
Coffee Break

Session IV: Metrology/Toolings

10:35-10:55
*Metrology Issues and Requirements for Novel Approaches to Nanomanufacturing
Gregg Gallatin
NIST

10:55-11:15
*Extension use of Immersion Lithography for the 22nm Half-pitch and Beyond
Rajit Kanaya
Nikon Precision China

11:15-11:35
*Cymer LPP EUV source system development status
Benjamin Szu-Min Lin1, Bruno La Fontaine1, David Brandt2, Nigel Farrar2

11:35-11:55
*300mm Wafer Stepper for Advanced package application
Chang Zhou
SMEE

11:55-12:15
Technology and Economic Considerations for High Volume HB-LED Lithography Manufacturing
Marathe Ranjan, Alex Chow
Ultratech

12:15-13:15
Lunch

** Keynote       * Invited
<table>
<thead>
<tr>
<th>Session V: Resist</th>
<th>Session VI: Process</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>13:20-13:40</strong></td>
<td><strong>15:30-15:50</strong></td>
</tr>
<tr>
<td><em>Foundry Efficiency Gains Through Common Photolithography Themes</em></td>
<td></td>
</tr>
<tr>
<td>James E Lamb III*, Chris Cox, Zhimin Zhu, David Drain Brewer Science</td>
<td><em>Limit of Line End Shortening Correction under Single Exposure in 193 nm Immersion Lithography</em></td>
</tr>
<tr>
<td>13:40-14:00</td>
<td>Qiung Wu, Verne Xu, Michael Hao, Winnie Liu, Xuelong Shi, Yiming Gu SMIC</td>
</tr>
<tr>
<td><em>One-component Positive Chemically Amplified Molecular Glass Deep-UV Photoresists</em></td>
<td></td>
</tr>
<tr>
<td>Jinxing Yu, Jiamuan Zhang, Liyuan Wang Beijing Normal University</td>
<td><strong>15:50-16:10</strong></td>
</tr>
<tr>
<td>13:40-14:00</td>
<td>Advanced Implant Resist for Profile Control below 28 node technology</td>
</tr>
<tr>
<td><em>Use of DBARCs Beyond Implant</em></td>
<td></td>
</tr>
<tr>
<td>Carlton Washburn, Joyce Lowes, Alice Guerrero Brewer Science</td>
<td>Yoshihiro Yamamoto Dow Chemical</td>
</tr>
<tr>
<td>14:20-14:40</td>
<td><strong>16:10-16:30</strong></td>
</tr>
<tr>
<td><em>Development of Under Layer material for EUV Lithography</em></td>
<td></td>
</tr>
<tr>
<td>R. Sakamoto, N. Fujitani, T. Endo, R. Onishi, B.C. Ho Nissan Chemical</td>
<td>248nm Process Is Capable for sub 0.09µm Groundrules?</td>
</tr>
<tr>
<td>14:40-15:00</td>
<td>Lei Wang, Yufeng Tong, Xiaobo Guo, Honglin Meng, Bo Su, Shian'an Xiao Huahong NEC</td>
</tr>
<tr>
<td>Advanced NTD Immersion Technology below 28nm Node Process</td>
<td></td>
</tr>
<tr>
<td>Xiaoming Ma Dow Chemical</td>
<td><strong>16:30-16:50</strong></td>
</tr>
<tr>
<td><strong>15:00-15:20</strong></td>
<td>Study to Transfer 0.11µm DRAM Litho ArF Process to KrF Process</td>
</tr>
<tr>
<td>Evaluation of 193nm Photoresist Material at Advanced Immersion Nodes</td>
<td></td>
</tr>
<tr>
<td>Michael Hao, Verne Xu, Winnie Liu, Qiung Wu, Xuelong Shi, Yiming Gu SMIC</td>
<td>Joe Liu, Eric Yao, Eric Fan, Kent Chang, Ted Li, Jief Zhang, Lee Liang, Jerry Hong SMIC</td>
</tr>
<tr>
<td><strong>15:20-15:40</strong></td>
<td><strong>16:50-17:10</strong></td>
</tr>
<tr>
<td>Coffee Break</td>
<td>Studying Photoresist Type for Sub-32nm Node Dense SRAM 2nd GT Layer</td>
</tr>
<tr>
<td></td>
<td>Verne Xu, Michael Hao, Winnie Liu, Xuelong Shi, Qiung Wu, Yiming Gu SMIC</td>
</tr>
</tbody>
</table>
Symposium III: Dry & Wet Etch and Clean

**Keynote**

**Invited**

**Symposium Chairs:**

Ying Zhang  
Manager, IBM, USA

Yue Kuo  
Prof., Texas A&M University

Tom Ni  
AMEC China

Jinrong Zhao  
VP, North Microelectronics, China

Maxime Darnon  
French institute for scientific research (CNRS)

Sebastian Engellmann  
IBM TJ Watson Research Center, USA

Masahiro Suniya  
Hitachi High-Technologies Corp., Japan

Denis Shamiryan  
Senior Scientist, IMEC

Li-Hung Chen  
Assist BU manager

Sunday, March 13

Session I: Front End Of Line (FEOL) Etching

Session chairs: Maxime Darnon, CNRS/LETI

13:15-13:20  
Chairman Remarks

13:20-13:55  
**Interest of Synchronized Pulsed Plasmas for Next CMOS Technologies**  
O. Joubert¹, M. Darnon¹, G. Cunge¹, E. Pargon¹, L. Vallier¹, N. Sadeghi¹, T. David¹, M. Haas¹, P. Bostard¹, C. Petit Étienne¹, S. Banno¹, T. Lill¹  
¹. LTM-CNRS, France; ². CEA-LETI, France; ³. Applied Materials, USA

13:55-14:25  
**Selective Removal of High-k Dielectrics**  
D. Shamiryan and V. Paraschiv  
IMEC, Belgium

14:25-14:40  
Active Area Width and Topography Effects on Sub 45nm Poly gate CD  
Man-Hua Shen, Xiao-Ying Meng, Yi Huang, Hai-Yang Zhang, Shih-Mou Chang, Kwok-Fung Lee, Yi-Ming Gu  
SMIC

14:40-14:55  
Silicon recess Investigation on Gate Plasma Etching for 40nm Technology and Beyond  
Song Huang  
Lam Research Corp, China

14:55-15:10  
**Reverse Phase Solution for Mesa Chamber Uniformity Improvement**  
Qing Ge, Xiaoduo Tang, Ying Huang  
Applied Materials, China

15:10-16:30  
Coffee Break

Session II: Back End Of Line (BEOL) Etching (I)

Session chairs: Tom Ni, AMEC

15:30-16:00  
**Plasma Etch Challenges for Porous Low k Materials for 32nm and Beyond**  
Cathérine Labelle¹, J. Arnot², Y. Yin³, R. Srivastava³, H. Yusuf³, J. Linville³, A. Darak⁴, K. Zhou⁴, V. Zhou⁴, J. Perdier⁴  
¹. GLOBALFOUNDRIES; ². IBM Research; ³. GLOBALFOUNDRIES Singapore; ⁴. IBM Microelectronics; ⁵. Applied Materials

Monday, March 14

Session III: Wet Etch and Clean

Session chairs: Li-Hung Chen, TEL

08:20-08:35  
**Dummy Ply Silicon Gate Removal by Wet Chemical Etching**  
T. Yang, H. X. Yin, Q. S. Xu, C. Zhao, Integrated Circuit Advanced Process Center (ICAC), Institute of Microelectronics Chinese Academy of Sciences, China

08:35-09:10  
**Cleaning Challenges and Solutions for Advanced Technology Nodes**  
Paul W. Mertens  
IMEC, Heverlee

09:10-09:25  
**Theoretical and Experimental Development of Advanced Dopant-Sensitive Systems**  
Peng Lin-da Zhang  
1. Qingdao Feiyang Vocational & Technical College, China;  
2. Jiangnan Planarization Equipment Limited Corp., China

09:25-09:55  
**Ultrapure Water-Related Problems and Waterless Cleaning Challenges**  
Takeshi Hattori  
Hattori Consulting International/Hanyang University

9:55-10:15  
Coffee Break
**Session IV: Plasma Etch Challenges**
Session chairs: Ying Zhang

10:15-10:45
*Ultimate Top-down Processes for Future Nanoscale Devices*
Seiji Samukawa, Tohoku University, Japan

10:45-11:00
Dry Etch fin Patterning of a sub 22nm node SRAM Cell: EUV Lithography New Dry Etch Challenges
E. Allamirano-Sánchez, Y. Yamaguchi, J. Lintan, H. Horiguchi, M. Ericken, M. Demand, W. Boullart
1. IMEC, Belgium; 2. Lam Research, Fremont California, US.

11:00-11:30
*TBD*
Thorsten Lill, Applied Materials, USA

11:30-11:55
Research on Etching of Diamond Films by ICP Oxygen Plasma
Wang Shasha, Zhang Taofeng, Ren Jun, Zhang Kaikang*
School of Electronics Information Engineering, Tianjin University of Technology, China

11:55-13:15
Lunch

**Session V: BEOL/MOL (II)**
Session chairs: Shamiryan Denis, IMEC

13:15-13:30
TBD
Posseme 1

13:30-13:45
Plasma Etching Parameters Impact to Low-k Damage
Jinhong Zhang, Hua Yuan Pei, LH Cheng, Sam Zhou, Steven Zhang, Morris Chang
Lam research (Shanghai) Co., Ltd

13:45-14:00
State of the art dielectric etch technology
Koichi Yatsuda, TEL, Japan

14:00-14:15
Prevention of Al/Cu line Galvanic Corrosion after Fluoride containing Stripper Cleaning: a case study
Bing Liu, Libbert Peng, Andrew Wang, Justin Sun
Anji Microelectronics (Shanghai) Co., Ltd, China

14:15-14:30
Highly Elective Etching Solutions for Advanced Logic Technologies
Xin-Peng Wang, Hai-Yang Zhang, Shih-Mou Chang, Kwok-Fung Lee, Xiaoming Yin
SMIC

14:30-14:45
The study of Contact CD Shrinkage on deep Sub-micron Technology
Jing-ying Huang, Qu-hua Han, Xin-peng Wang, Elaine Zhang, Shih-Mou Chang, Kwok-Fung Lee
SMIC

14:45-15:05
Coffee Break

**Session VI: Metrology, Resist Strip and Other applications**
Session chairs: Jingrong Zhao, North Microelectronics

15:05-15:25
Sensor Wafers for Plasma Etching
A.P. Milkinin, M. Demand, W. Boullart, P. Arleo
1. IMEC, Belgium; 2. KLA-Tencor, USA

15:25-15:30
Study on Si Sieve Holes Array for Future Lithography Application
Weihua Si, Ming Yin, Jun Gai, Zemin Liu*
1. Tsinghua University, China; 2. Hunan University, China

15:45-15:55
Low Si and SiGe Loss in High Dose Implant Resist Strip
Xiao-Ying Meng, Man-Hua Shen, Yi Huang, Hai-Yang Zhang, Shih-Mou Chang, Kwok-Fung Lee
SMIC, China

15:55-16:15
Effluent Management for Non-Oxidizing Plasma Strip Processes
Shijian Luo, Carlo Waldhied, Orlando Escorcia, Ivan Berry, Philip Geisbuhler, LGA

16:15-16:30
Wafer Backside Particle Reduction By Optimizing AC3 Coating for Poly Etch Chamber
B. Ma, W. Liu, F. Niu
LAM

**Keynote**  * Invited
## Symposium IV: Thin Film Technologies

### Symposium Chairs:
- Jionping Lu  
  Director, SMIC, China
- WeiE Wang  
  Intel assignee at IMEC, Belgium
- Zhen Guo  
  Technology, Intel, USA
- Jason Tian  
  VP, Nikon Precision, China
- Jon Reid  
  Fellow, Novellus, USA
- YuLong Jiang  
  Fudan University, China
- Xiaoping Shi  
  IMEC, Belgium
- Duofeng Yue  
  TI, USA
- Kyoichi Sugii  
  Toshiba, Japan
- YuLong Jiang  
  Fudan University, China
- Jason Tian  
  Nikon Precision, China

### Sunday, March 13

#### Session I: FEOL - 1

13:15-13:20  
**Chairman Remarks**

13:20-13:45  
**Research on Non-silicon High-mobility Channel Materials for Future High Speed and Low Power Logic Transistors**  
Willy Rachmady  
Intel, USA

13:45-14:10  
**Evolution of Thin Film Epitaxial Technologies for Sub-32nm Advanced Logic Applications**  
Sathwesh Kappurao  
Applied Materials

14:10-14:35  
**Electron States at Interfaces of Semiconductors and Metals with Insulating Films**  
V. V. Afanas’ev, M. Houssa, A. Stesmans  
University of Leuven, Belgium

14:35-15:00  
**Selective Epitaxial Growth: Trends in a Modern Transistor Device Fabrication.**  
A. Hikavyy, W. Vanherle, B. Vincent, J. Dekoster, L. Witters, T. Hoffman, R. Loo  
IMEC, Belgium

15:00-15:20  
**TBD**  
Moinpour, Mansour  
Intel, USA

15:20-15:45  
**Coffee Break**

#### Session II: FEOL - 2

15:20-15:45  
**Electron States at Interfaces of Semiconductors and Metals with Insulating Films**  
V. V. Afanas’ev, M. Houssa, A. Stesmans  
University of Leuven, Belgium

15:45-16:10  
**Rare Earth Aluminate Thin Films for Non-volatile Memory Applications**  
Christoph Adelmann  
IMEC, Belgium

16:10-16:30  
**Evolution of STI gap fill technology**  
James C Chen, Yingjie Chen, Rong Guo, Charley Cheng, Xiaoyuan Li, Guangming Zhao, Terrace Lee  
1. Applied Materials China; 2. Applied Materials

### Monday, March 14

#### Session III: BEOL & 3D Interconnection - 1

08:15-08:40  
**Challenges of Aggressive Scaling of Low-k Materials**  
Mikhail Baklanov  
IMEC, Belgium

08:40-09:05  
**PECVD Applications for 32nm and Beyond**  
Pramod Subramonium  
Novellus systems

09:05-09:30  
**ALD Ru and its Applications in DRAM MIM-Capacitors and Interconnect**  
Marc Schaeckers, Johan Swerts, Laith Altimime, Zsolt T kei  
IMEC, Belgium

09:55-10:15  
**Evaluation of Metallization Options for Advanced Copper Interconnects Application**  
Nicolas Jourdan  
IMEC, Belgium

10:15-10:40  
**Technology Options for Reducing Contact Resistances in Sub-22nm Transistors**  
Yee-Chia yeo  
National University of Singapore

10:40-11:05  
**Gap Filling Processes for High AR Structures**  
Zhan Chao  
IMECAS

**Keynote**  
* Invited
11:00-11:30
*Fine Pitch Micro-bump Interconnections for Advanced 3D Chip
W. Zhang, P. Limaye, A. La Manna, P. Soussan IMEC, Belgium
11:30-11:50
Temperature and Stress Effects on the IMC Behavior of Thin Film Cu-Al System in Wire Bond
Xuefei Ming, KunQuan Fan
1. CETC No.58 Research Institute; 2. ASM Pacific Technology, Singapore
11:50-13:15
Lunch

Session V: Nano, Solar and Novel Materials - 1

13:15-13:40
*Applications of Atomic Layer Deposition for Nanoscale Devices and Other Emerging Applications
Hyungjun Kim Yonsei University
13:40-14:05
*Review of Silicon nanowire Oxidation
X. Shi, R. Kurstjens, I. Vos, J-L. Everaert, M. Schaekers IMEC, Belgium
14:05-14:30
*Low cost Solution-processed High-k Gate Dielectric Materials for Large Area Applications
Wan-Yu Lin, Robert Muller, Soeren Steudel, Kris Myny, Jan Genoe, Paul Heremans IMEC, Belgium
14:30-14:50
Effect of Gate Length on the Transconductance of Graphene Nanoribbon Field Effect Transistors (GNRFETs)
14:50-15:10
Effect of Film Thickness on Resistance Switching Characteristics for Cu/NiO/Pt Structure
Zhang Yang, Wang Fang Wei Xiaoqing, Wang Qi, Zhang Kaiqiang Tianjin University of Technology
15:10-15:30
Coffee Break
Symposium V: CMP and Post-CMP Cleaning

Symposium Chairs:
Ara Philipossian  
Shumin Wang  
Charles Xing  
Jingxun Fang  
Kailiang Zhang  
Kuochun Wu  
Mahadevaiyer Krishnan  
Gary Ding  
Weichung Yu  
Paul-Chang Lin  
David Huang  
Takenao Nemoto  
Yohei Yamada

Program:
16:35-16:55
Investigation on the Correlationship between Process Performances and Composition of CMP Slurry Designed for GST Alloy Polishing
Keliang Pang  
Anji Microelectronics (Shanghai) Co., Ltd.

Session III: Fundamentals
8:30-8:55
*Functionalized Silica Abrasive-based Dispersions for Tunable Polishing of Polysilicon over Silicon Dioxide/silicon Nitride Films
P.R. Dhand Vearra, Navesh K. Penta, S.V. Babu*
Center for Advanced Materials Processing, Clarkson University, USA

9:00-9:20
*Fundamental Characterization Studies of Condensed Chemical Mechanical Polishing Waste Slurry
Yohei Yamada, Masanori Kawakubo, Takahiro Sugaya, Shusuke Watanabe
Micro Device Division, Hitachi, Ltd., Japan

9:20-9:40
Correlation of Pad Topography, Friction Force and Removal Rate during Tungsten Chemical Mechanical Planarization
Ara Philipossian  
Robert Rhoades  
Kailiang Zhang  
Weichung Yu  
Weili Liu  
Tadahiro Ohmi  
Takenao Nemoto  
Ara Philipossian  
Yasa Sampurno  
1. Tohoku University, Japan; 2. Araca, Inc., USA; 3. University of Arizona, USA

9:40-10:00
Effect of Mechanical Process Parameters on Friction Behavior and Material Removal during Sapphire Chemical Mechanical Polishing
Zefang Zhang  
Weili Liu  
Zhitang Song  
1. Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, China; 2. Graduate School of the Chinese Academy of Sciences, China; 3. Shanghai Xitana Electronic Science & Technology Co., Ltd., China

10:00-10:20
Coffee Break

Session IV: Modeling
10:20-10:45
*Tribological and Kinetical Analysis of Barrier Metal Polishing for Next Generation Copper interconnects
Ricardo Duyos-Mateo  
Xun Gu  
Takenao Nemoto  
Yasa Sampurno  
Ara Philipossian  
Adrian Rice  
Yun Zhuang  
1. Tohoku University, Japan; 2. Araca, Inc., USA; 3. University of Arizona, USA

10:45-11:05
Finite Element Analysis (FEA) of Pad Deformation Due to Diamond Disc Conditioning in Chemical Mechanical Polishing (CMP)
Emmanuel A. Baisie  
Bin Liu  
Xiaohong Zhang  
1. North Carolina Agricultural & Technical State University, USA; 2. Tianjin University, Tianjin, China; 3. Seagate Technology, Minneapolis, Minnesota, USA

* Keynote  * Invited
11:05-11:25
**Mathematical Models to Predict Pad Surface Profile Resulted from Diamond Disc Conditioning in Chemical Mechanical Polishing (CMP)**
Emmanuel A. Baisie, Z.C. Li, Bin Lin, Xichong Zhang
1. North Carolina Agricultural & Technical State University, USA;
2. Tianjin University, Tianjin, China; 3. Seagate Technology, Minneapolis, Minnesota, USA

11:25-11:45
Data Driven CMP Manufacturing Modeling for Process and Design Optimization
Lj J Song Ph.D., Vikas Mehrotra Ph.D.
Ascertin LLC, Fremont, CA, USA

11:45-13:15
Lunch

Session V: Processes

13:15-13:40
*Ge- and III/V-CMP for Integration of High Mobility Channel Materials*
Patrick Ong, Liesbeth Witters, Niamh Waldron, Peter Leunissen
IMEC, Belgium

13:40-14:00
Advanced Direct-polish Process on Novel Non-porous Ultra Low-k Fluorocarbon Dielectric on Cu Interconnects
Xun Gu, Takenao Nemoto2, Yuya Tomita, Ricardo Duyos-Mateo*, Akinobu Teramoto2, Shin-Ichiro Kuroki1, Shigetoshi Sugawa1, Tadahiro Ohmi2
1. Graduate School of Engineering, Tohoku University, Japan;
2. New Industry Creation Hatchery Center, Tohoku University, Japan

14:00-14:20
Floating Gate CMP Poly Residue and Big AA Poly Dishing Performance Study
Jack Zhang, Cindy Li, Lily Jiang, Feng Chen
SMIC

14:20-14:40
Effect of Slurry Application/Injection Methods and Polishing Conditions on Bow Wave Characteristics
Ara Philipossian1, Xiaoyan Liao2, Yasa Sampurno1,2, Yun Zhuang1,2, Fransisca Sudarigo1, Adam Rice2
1. Araca, Inc., USA; 2. University of Arizona, USA

14:40-15:00
Coffee Break

Session VI: Defect Reduction

15:00-15:25
*Evolution of Post CMP Cleaning Technology*
Gautam Banerjee
Air Products and Chemicals, Inc.

15:25-15:50
*Cleaning Aspects of Novel Materials after CMP*
Rita Vos
IMEC

15:50-16:15
*A Novel Approach for More Effective Wafer Edge Post-CMP Cleaning*
R.K. Singh, C. Patel, D. Trio, E. McNamara and C.R. Wargo
Entegris, Inc., USA

16:15-16:35
Study on the Ring Type Crater Defect Reduction in Cu CMP Process
Jin-Hai Xu1, Paul-Chang Lin1,2, Charles Xing1,2, Wei Li1, Zhi-Yong Ma1
1. SMIC; 2. Department of Microelectronics and Solid State Electronics, Fudan University

16:35-16:55
New Application of Optical Endpoint System: In situ Cu Residue Detection
Weifeng Zhang1, Xucheng Wang1, Changping Tan1, Shan Wang1, Walters Shen1, George Ge3

---

**Keynote**  * Invited
Symposium VI: Materials and Process Integration for Device and Interconnection

Symposium Chairs:
- Ran Liu, Professor, Fudan University, China
- Frank Chen, Director, SMIC, China
- Sowmya Krishnan, SEMITRAC, USA
- Massayasu Tanjyo, Nissin Ion Equipment
- Gamming Zhao, Technical Director, Applied Materials
- Zheyao Wang, Professor, Tsinghua University, China
- Archie Liao, Asia EFP Technology Manager, Air Products, China
- Da Zhang, Member of Technical Staff, Freescale
- Larry Zhao, Intel

** Keynote * Invited

Session I: Process Integration for Device - I

Sunday, March 13

13:15-13:20
Chairman Remarks
Jing Li, IBM Watson Research Center

13:20-13:45
*Phase Change Memory Circuits
Jing Li, IBM Watson Research Center

13:45-14:05
SiON Gate Dielectric Optimization for NBTI Improvement
Yonggen He, Li Wen, Wenbo Wang, Rui Guo, Youfeng He, Yonggen He, Sean F Zhang, Jianhua Ju
SMIC Beijing

14:05-14:25
Analysis of the Temperature Dependence of Trap-Assisted-Tunneling in Ge pFETs Junctions
M.B. Gonzalez, G. Eneman, B. De Jaeger, E. Simoen, C. Claeyssen
1. IMEC, Belgium; 2. EE Dept., KU Leuven, Belgium; 3. Research Foundation-Flanders

14:25-14:45
e-SiGe Global and Micro Loading Effect Investigation for High Performance CMOS Manufacture
Yonggen He, Youfeng He, Huojin Tu, Shanshan Du, Huatong Song, Jing Lin, Tzu-Chiang Yu, Jingang Wu
SMIC Shanghai

14:45-15:05
WCVD Nucleation RS Uniformity Optimization for 0.13um Logic Product Cp Improvement
Fei Zhong, Paul-Chang Lin, Zhi-Chao Li, Dong-Du Yang, Jian-Yong Jiang, Yi-Hui Lin
1. Shanghai Jiao Tong University; 2. Fudan University

15:05-15:20
Coffee Break

Session II: Process Technology - I

15:20-15:45
*Overview on MG/HK
Tom Schram, IMEC, Belgium

15:45-16:10
*TBD
Yasuhi Akiyama, TEL

16:10-16:30
Investigation of Ni-based Silicide Formation by Different Dynamic Surface Annealing Approaches
Yonggen He, Bing Wu, Guobin Yu, Jin Lin, Sean Zhang, Jiong-Ping Lu, Jingsong Wu, Jiuyi Tang, Gamming Zhao
1. SMIC Shanghai; 2. Applied Materials China

16:30-16:50
Robust Shallow Trench Isolation High Density Plasma Chemical Vapor Deposition Void Free Process for 0.13um CMOS Technology
Grace Ning, Paul-Chang Lin, Charles Xing, Allen Bian, Hong-Bo Zhao, Yi-Lu Cao
1. SMIC Shanghai, PRC; 2. Fudan University

16:55-17:10
Spacetime-dependent diffusion
Xiao-Fan Chen, Harbin Institute of Technology, China

Monday, March 14

Session III: Process Integration for Device - II

8:30-8:55
*Phase Change Memory Device
Chung Lam, IBM Watson Research Center

8:55-9:20
*Conduction Mechanism of Metal Oxide (HfOx) - Based RRAM Devices: A Comprehensive Study
Hong-Yu Yu, Nanyang Technological University

9:20-9:40
Epoxy – Ba0.5Sr0.5TiO3 Composites for Embedded Capacitor Applications
Seok-Woo Yun, Yong-Jun Park, Jung-Hyuk Koh, Kwangwoon Univ., Seoul, Korea

9:40-10:00
CMIFless Planarization Technology with LTO/SOG Etchback for Low Cost 70nm Gate-Last Process
Haixiang Yin, Lingkuan Men, Tao Yang, Gaobo Xu, Qiuxia Xu, Chao Zhao, Daping Chen Institute of Microelectronics, Chinese Academy of Sciences

10:05-10:20
Coffee Break

Session IV: Process Technology - II

10:20-10:45
*Etch and Clean Challenges and Joint Optimization
BMing Yen, Lam Research

10:45-11:10
*Growth and processing defects in CMOS hetero-epitaxy
Eddy Simoen, IMEC, Belgium

11:10-11:30
Precise Control of Spike Anneal Process for Advanced CMOS
Zhizhao Zhao, Ji Yue Tang, Gamming Zhao, Applied Materials China

http://semiconchina.semi.org/cstic
Session V: Process Integration for Interconnect
13:15-13:40
*Interconnect Scaling Trends and Opportunities
Satya V. Nitta  IBM, USA

13:40-14:00
Improving Copper Interconnect Reliability via Ta/Ti Based Barrier
Xiao-Wen Hu, Paul-Chang Lin, Jian-Yong Jiang, Peng He
1. SMIC, Shanghai; 2. Fudan University

14:00-14:20
Glue Layer Study of Inter Via between Cu and Al Metal Lines
John Chen  SMIC

14:20-14:40
The Influence of The SiN Cap Process on The Voltage Breakdown and Electromigration Performance of Cu interconnects
Ya-Lu Cao, Paul-Chang Lin, Charles Xing, Allen Bian, Neil Xu
1. SMIC, Shanghai; 2. Fudan University

14:40-15:00
Effect of RF Power on Carbon Nanotubes Synthesized at Low Temperature by RF-PECVD
Lin Xinyuan, Hu Kai, Caiqiai Xiaoyong, Wang Shiwei and Zhang Kailiang
Tianjin University of Technology, China

15:00-15:15
Coffee Break

Session VI: Process Technology - III
15:15-15:40
*Process Characterization of Low Temperature Ion Implantation Using Tall Beam and Spot Beam
Hank Chen, Erik J.H. Collart, M.A. Razali, Russell Gwilliam, Andy Smith
1. Advanced Ion Beam Technology, Inc.; 2. University of Surrey

15:40-16:00
Laser Solution for ITO Patterning Processing
Chunhao Li  Shinecon Laser Co.

16:00-16:20
Polymer Solar Cells
Jie Liu  Ysolars

16:20-16:40
Improving Yield with High-Performance Cables
Paul Warren  W. L. Gore & Associates, Inc.

16:40-17:00
Reliability Study of Fast Curing Isotropic Conductive Adhesive
Wenhui Du  Shanghai university

17:00-17:20
Effect of Functionalization of Silver on Rheological and Electrical Properties of Conductive Adhesives
Qiong Fan, Huawang Cui, Johan Liu
1. Shanghai University, China;
2. Shanghai University, China;
3. Chalmers University of Technology, Sweden;
4. SIHT Smart High Tech AB
Symposium VII: Packaging and Assembly

Session I: 3D Packaging
Session Chair: Tom Jiang
13:15-13:20
Chairman Remarks
13:20-13:50
3D System Integration - Opportunities and challenges
Eric Beyne IMEC
13:50-14:20
An Electronic Material Supplier’s perspective on Challenges and Opportunities in 3D Packaging
Leo Linhan Dow Electronic Materials
14:20-14:55
TBD
Calvin Cheung ASE
14:55-15:05
Future Trends in Multi-dimensional Stacked Packaging
Robert Yang Telesis
15:05-15:25
Coffee Break

Session II: Advanced Packaging
15:25-15:55
Electronics Product Miniaturization and Reliability
Dongkei Shangguan Flextronics
15:55-16:20
TBD
Lei Shi Nan tong Fujitsu
16:20-16:45
High Speed IC Package Design Considerations
Zhang Tonglong Statschippac China
16:45-17:05
Geometric Effect on the Performance of Heatsink Containing Microchannels
Jiqun Jia* , Han-Chieh Chiu* , Chia-Jui Yang† 1. Ming Chi University of Technology; 2. Technology and Science Institute of Northern Taiwan, China

Monday, March 14

Session III: Packaging Materials
8:30-9:00
Nano Materials and Nanocomposites for Advanced Electronic and Photonic Packaging Applications
Dr. C. P. Wong Georgia Institute of Technology
9:00-9:25
Pb-free Solder Materials and Technology
Young-Me Kim Hanyang University
9:25-9:55
TIW Acts as a Barrier to Cushion the Copper Wire Bonding Force and Preventing Underneath Silicon Damage
Lai chin yung ON Semiconductor
9:55-10:10
Microstructural Evolution and Its Effects on Properties of SnAgCu Bi Cr/Cu Lead-free Solder Joints During Thermal Aging
Fei Lin, Yongjiu Han, Wenzhen Bi, Xicheng Wei Shanghai University
10:10-10:30
Coffee Break

Session IV: Interconnection
10:30-10:55
Study of EMC for Cu Bonding Wire Application
Toshiro Takeda Sumitomo Bakelite Co., Ltd.
10:55-11:10
Influence of Process Parameters on the Performance of a Novel Anisotropic Conductive Adhesive in Lead-free Assembly
S. Manian Ranikumar*, Hari Venugopalan*, Kumar Khanna2 1. Rochester Institute of Technology, USA; 2. SunRay Scientific, USA
11:10-11:30
Corrosion of Gold and Copper Ball Bonds
C. D. Breach1, Hun Shen Ng2, Teck Kheng Lee2, R. Holliday3 1. ProMat Consultants, Singapore; 2. ITE College Central, Singapore; 3. World Gold Council, UK
11:30-11:50
Cost-effective Use of Gold Wire in Semiconductor Packaging
11:50-12:10
Copper Wire Bonding in High Volume Manufacturing
Bernd K Appelt, Andy Tseng, Yi-Shao Lai, Chun-Hsiung Chen ASE Group
12:10-13:15
Lunch
Session V: Process Technologies

13:15-13:45
MUF Technology Development for SiP Module
YoungDo Kweon*, Joo Hae Ko, KiChan Kim, MinGook Jang, JaeCheon Doh, ChangBae Lee, DoJae Yoo
Samsung Electro-Mechanics Co., LTD

13:45-14:05
Multi Beam Grooving and Full Cut Laser Dicing of IC Wafers
Jeroen van Borkulo, Rene Hendriks
ALSI

14:05-14:25
Advanced Bump Structure for Improving the Board Level Characteristics of WLCSP
ChangBae Lee*, Jongwoo Choi, Jin-Su Kim, Sangmoon Choi, Dojae Yoo, Seungwook Park, Youngdo Kweon
Samsung Electro-Mechanics Co., LTD

14:25-14:40
Plasma Cleaning Effect on Automotive Devices
Chew Pei Yi
Infineon

14:40-14:50 Coffee Break

Session VI: Packages and Characterizations

14:50-15:05
TBD
Herb Huang
SMIC

15:05-15:25
An Investigation of Thermal Management Design for High Brightness LED Array Package on PCB
KC Yung, H Liem, HS Choy
The Hong Kong Polytechnic University

15:25-15:50
Packaging Issues of High Voltage Power Modules
S. S. Ang, T. Evans, J. Zhou, K. Schmier, H. Zhang, B. Rawdon, J. C. Balda, H. A. Mantooth
University of Arkansas

15:50-16:10
UV Curable Resin for Making High Reliability Image Sensor Package
Taro Kenmochi
Kyoritsu Chemical & Co., Ltd.
Symposium VIII: Metrology, Reliability and Testing

Symposium Chairs:
- Peilin Song, Manager, IBM, USA
- Bin Wang, Spansion, China
- Wen-ii Wu, Fellow, NIST, USA
- Yuhua Cheng, Peking University, China
- Francis Jen, Technical Director, KLA-Tencor, China
- Kelvin Xia, Manager, Verigy, China
- Srinivas Raghvendra, Synopsys
- Xiaowei Li, Institute of Computing Technology, Chinese Academy of Sciences
- Yu Huang, Sr. Research Staff member, Mentor Graphics, USA
- Qiang Guo, Director, SMIC
- Jian-fu Zhang, Prof. of Microelectronics in the School of Engineering, Liverpool John Moores University

Sunday, March 13

Session I: Testing

13:00-13:05
Chairman Remarks

13:05-13:35
** Testing

IDDDQ test Practice in Nanotechnologies
Samuel Ye, Clayton Shen, Jane Liu, Availink, Inc.

Cost-effective Solution for Jitter Performance Test in High-Speed Serial Links
Ming Lu, Verigy (Shanghai) Co., Ltd

Fault Isolation Along Address Line for FPGA Device Using Nanoprobing and Focused-Ion-Beam
Caiwen Yuan, Altera Corporation

Fault Isolation in FPGA Using Lock-in Thermography
Caiwen Yuan, Altera Corporation

Coffee Break

Session II: Yield and Failure Analysis

15:15-15:40
*Testing
Ting-Pu Tai, Mentor Graphics, USA

Spatial and Statistical Analysis of Wafer Test Data with R
Brian L. Ji, University at Albany-State University of New York, USA

A New LVS Method for Yield Analysis Chip
SHEN Fei, SHI Zheng, PAN Wei-wei, YAN Xiao-ting, VLSI Institute of Zhejiang University

16:25-16:45
Plasma Etching for Failure Analysis of Integrated Circuit Packages
J. Tang, J.B.J. Schaken, C.I.M. Beenakker, Delft University of Technology

16:45-17:05
Process Optimization of Contact Module in NOR Flash Using High Resolution e-Beam Inspection
Hsiang-Chou Liao, Che-Lun Hung, Tsung-Luch*, Ling-Wu Yang, Tahnone Yang, Kuang-Chao Chen, Chih-Yuan Lu, Macronix International Co. Ltd.

Monday, March 14

Session III: Metrology - I

8:15-8:45
**X-ray Metrology for Future Nano Sciences and Technologies
Kenji Saku i, National Institute for Material Science, Japan

Critical Dimension Measurement of line gratings using Specular X-ray Reflectivity – The coherence length effect and Its Measurement
Hae-Jeong Lee, Christopher L. Soles, Wen-li Wu, NIST, USA

9:05-9:25
Relative Calibration For Cross-Fab Alignment
Shun Jiang, Mark Zhang, Ming Li, Frank Yang, Nici Fan, Kaily Cao, SMIC, China

9:45-10:05
TSV/3D-IC Profile Metrology based on IR-Microscope Image
Jing-Jou Tang, Lien-Yong Lin, Li-Shyang Chen, Southern Taiwan University, National Cheng Kung University

10:05-10:25
Coffee Break

Session IV: Metrology - II

10:25-10:50
*Metrology
Weibing Yun, Xradia, USA

10:50-11:10
Endpoint Detection in Plasma Etching using Principal Component Analysis and Expanded Hidden Markov Model
Seung-Kyun Kim, Min-Woo Kim, Shu-Kun Zhao, Sang Jeon Hong, Seung-Soo Han, Myongji University, South Korea

** Keynote  * Invited
### Conference Agenda

**Keynote** * Invited

**Session V: Reliability - I**

<table>
<thead>
<tr>
<th>Time</th>
<th>Title</th>
<th>Speaker(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>11:10-11:30</td>
<td>Improvement of In-line OpticalCD Metrology on BEOL Copper CMP Erosion Layers for 65nm Technology Node Logic Production</td>
<td>Jolly Zhao¹, Clear Rong², Zhengchao Yin²</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1. KLA-Tencor China; 2. Semiconductor Manufacturing International Corp</td>
</tr>
<tr>
<td>11:30-11:50</td>
<td>Spectral Sensitivity Analysis of OCD based on Muller Matrix Formulism</td>
<td>Shi Yaoming¹, Zhang Zhengheng¹, Liu Guoxiang¹, Liu Zhijun¹, Xu Ying²</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Raintree Scientific Instrument (Shanghai) Corporation</td>
</tr>
<tr>
<td>11:50-12:10</td>
<td>A Method to Determine Process Capability Cpk and Corresponding OOS Probability for Non-normally Distributed and Limited Production Data</td>
<td>Siyuan Frank Yang¹</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12:10-13:20</td>
<td>Lunch</td>
<td></td>
</tr>
</tbody>
</table>

**Session V: Reliability - I**

<table>
<thead>
<tr>
<th>Time</th>
<th>Title</th>
<th>Speaker(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>13:20-13:50</td>
<td><strong>Reliability</strong></td>
<td>Carole Graas IBM Corp., USA</td>
</tr>
<tr>
<td>14:10-14:30</td>
<td>The Degradation Mechanism in Electrical and Optical Characteristics of High Power Light Emitting Diodes</td>
<td>KC Yung¹, HS Choy¹, Department of Industrial and Systems Engineering, The Hong Kong Polytechnic University</td>
</tr>
<tr>
<td>14:30-14:50</td>
<td>Adhesion and Shunting Effects of Barrier Layers on Reliability of Cu Interconnects</td>
<td>Yan Ju Yu¹, Qiang Guo¹, Jeff Wu¹</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SMIC, China</td>
</tr>
<tr>
<td>14:50-15:10</td>
<td>Study the Mixed-mode Delamination of the Epoxy/Cu Interface</td>
<td>Yu Liu¹, Jun Wang¹, Fudan University</td>
</tr>
<tr>
<td>15:10-15:20</td>
<td>Coffee Break</td>
<td></td>
</tr>
</tbody>
</table>

### Session VI: Reliability - II

<table>
<thead>
<tr>
<th>Time</th>
<th>Title</th>
<th>Speaker(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:20-15:45</td>
<td>*Interconnect Reliability Challenges for 22nm Technology Node and Beyond</td>
<td>Larry Zhao¹, Kristof Craes², Chris Wilson³, Zsolt T Kei, Gerald Beyer, and Cor Claey² IMEC, Belgium</td>
</tr>
<tr>
<td>15:45-16:10</td>
<td>*TEM</td>
<td>Jinghong (John) Li¹, IBM Corp., USA</td>
</tr>
<tr>
<td>16:10-16:30</td>
<td>Thermal SOA Investigation of a Novel 800V Multiple RESURF LDMOS with Linear P-top Rings</td>
<td>Aloysius P. Hermans¹, Gene Sheu¹, Hitomo S. Wasisto</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Asia University, Taiwan</td>
</tr>
<tr>
<td>16:30-16:40</td>
<td>Investigation of Lateral Die Crack Failure on Green IC Package</td>
<td>Yuen Chun 301, Chin Meng 301, Xin Chen¹, Kok Yau Chu¹, Ruomin Mike Du Infinion Technologies (Wuxi) Co. Ltd</td>
</tr>
<tr>
<td>16:40-17:00</td>
<td>Reliability Methodology for Micro-accelerometer under Shock Load</td>
<td>Jia Yubin¹, Wang Shihao¹, Hao Yilong¹, Huang Qingwen²</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1. Institute of Microelectronics Peking University</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. the 5th Electronics Research Institute of the Ministry of Industry and Information Technology</td>
</tr>
<tr>
<td>17:00-17:30</td>
<td>A Study of the Evolvement of Fluorine Corrosion on the Aluminum Pad</td>
<td>Paul Yu¹, Ivy Duan¹, Yuke Wang¹</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SMIC, China</td>
</tr>
</tbody>
</table>
Symposium IX: Emerging Semiconductor Technologies

Symposium Chairs:
Qinghuang Lin  Sr. Scientist, IBM, USA.
Jia Chen  Research Staff Member, IBM, USA.
Edward Y. Chang  Professor, National Chiao Tung University, China
Jing Kong  Professor, MIT, USA
Hyungjun Kim  Associate Professor, Yonsei University
Jinn P. Chu  National Taiwan University of Science and Technology, China
Jie Zhang  Singapore
Fuhua Yang  Professor, Institute of Semiconductor,
Chinese Academy of Sciences, China
Wang Yueh  Intel, USA
Jing Kong  Professor, MIT, USA
Hyungjun Kim  Associate Professor, Yonsei University
Jinn P. Chu  National Taiwan University of Science and Technology, China
Jie Zhang  Singapore
Fuhua Yang  Professor, Institute of Semiconductor,
Chinese Academy of Sciences, China
Wang Yueh  Intel, USA
Paul R. Berger  Ohio State University, USA

Session I: Emerging Process technologies
13:00-13:05  Chairman Remarks
13:05-13:35  **High Resolution Patterning: a View of the Future
C. Grant Willson  The University of Texas, USA
13:35-14:00  *New Research Opportunities Enabled by Fabless Access to Advanced Technologies
Michael Fritze  USC Information Sciences Institute
14:00-14:25  *Organic Thin-films for Directed Assembly of Block Copolymer Materials
Padma Gopalan  University of Wisconsin-Madison
14:25-14:50  *Oxide Thin-Film Device Integration: a Barrierless Cu-based Metallization
Jinn P. Chu, C. H. Lin  National Taiwan University of Science and Technology
14:50-15:05  FPGA Design with Double-Gate Carbon Nanotube Transistors
M. Haykel Ben Jassem  Commissariat a l’Energie Atomique (CEA-LETI)
15:05-15:20  Coffee Break

Session II: Post Si CMOS Options
Session Chair: Edward Chang, National Chiao Tung University, China
15:20-15:50  **3D Integration
Takayuki Ohba  University of Tokyo
15:50-16:15  *Single-layered Planar Nanodevices for THz Imaging and Energy Harvesting
Aimin Song  University of Manchester

Session III: LEDs
8:30-9:00  **LED Overview
Decai Sun  Philips
9:00-9:25  *GaN-on-Si Power Devices and Light Emitting Diodes
Kai Cheng  IMEC
9:25-9:40  Vertical LED with DLC Interface for High-Power Illumination
Michael Sung  SinoDiamond LED
9:40-9:55  Enhancing GaInAs/GaAs Quantum Well Emission by Nanopatterned Silver Dots
N. Xiang, K. H. Tung, B. Z. Wang  1. National University of Singapore; 2. Institute of Materials Research and Engineering, Singapore
9:55-10:10  Alumina Abrasives for Sapphire Substrate Polishing
David Merricks  Ferro Electronic Material Systems, USA
10:10-10:25  A Thermal Study of BN Doped Epoxy Matrix PCB Materials for High Brightness LED Package
KC Yung, H. Liem, HS Choy  The Hong Kong Polytechnic University
10:25-10:45  Coffee Break

Session IV: Novel Materials, Processes and Applications-I
10:45-11:10  *Experimental and Modeling on Atomic Layer Deposition Al2O3/ n-InAs Metal-oxide-semiconductor Capacitor with Various Surface Treatments
E. Y. Chang  National Chiao Tung University

Sunday, March 13
Monday, March 14
**Keynote  Invited**

9

11:10-11:35  
*Magnetic behaviors of highly Mn-doped (Ga,Mn)As*
Jianhua Zhao  
Institute of Semiconductors, Chinese Academy of Sciences, China

11:35-11:50  
**Effects of Surface Pretreatments to p-GaN Substrate on Ohmic Contact of p-GaN/GZO and Lighting Performance of LED Chips**
Wangli Wang, Jianhua Zhang, Jinsong Zhang  
Shanghai University

11:50-12:05  
**A Phase Change Memory Device Fabrication Technology Using Si$_2$Sb$_2$Te$_6$ for Low Power Consumption Application**
Ying Li, Xudong Wan, Zhitang Song, Joseph Xie, Bo Liu, Guaping Wu, Nantie Zhu, Jia Xu, Min Zhong  
1. SMIC; 2. SIMIT, Chinese Academy of Sciences; 3. Microchip (Shanghai) Ltd

12:05-13:20  
Lunch

**Session V: Novel Materials, Processes and Applications-II**

13:20-13:45  
*Business units and core competences of Fraunhofer ENAS*
Thomas Gessner  
Fraunhofer Research Institution for Electronic Nano Systems ENAS

13:45-14:10  
*CNTs*
Chunming Niu  
Unidym

14:10-14:25  
**Effect of Carbon Nanotube diameter**
R. Yahyazadeh, Z. Hashempour  
Islamic Azad University

14:25-14:40  
**An Advanced 0.13µm Split-gate Embedded Flash Technology with High Reliability and Performance**
Chao Gao  
Grace Semiconductor Manufacturing Corporation

14:40-14:55  
**Benefits of Integrating Proven Materials for Semi Wafer Fabrication**
Garth Su  
Greene, Tweed

14:55-15:10  
Coffee Break

**Session VI: PV**

15:10-15:35  
*Transparent Conductive Oxide Doped for Thin Solar Cell Application*
Doyoung Kim, Hyungjun Kim  
Yonsei University

15:35-16:00  
**Electrical Characterization of the MOS (Metal-oxide-semiconductor) System: High Mobility Substrates**
Dennis Han-Chung Lin  
IMEC

16:00-16:15  
**Characterization of CdS Thin Films Grown by Chemical Bath Deposition**
Weibo Zhang, Shuying Cheng  
Fuzhou University

16:15-16:30  
**Polymer Solar Cells**
Jie Liu  
Ysolars

16:30-16:45  
**Electroluminescence of End-Capped Poly[9,9-di-(2'-ethylhexyl)fluorenyl-2,7-diy] Blended with F8BT**
Qiushu Zhang  
University of Electronic Science and Technology of China

16:45-17:00  
**Enhancement of Luminance via Blending F8BT with Tetraphenyldiaminobiphenyl-Containing Hole Transport Polyme**
Qiushu Zhang  
University of Electronic Science and Technology of China
Symposium X: Silicon Technology for Electronic and Photovoltaic Application

Session I: Silicon Materials and Wafer Processing
Session chairs: Mrs. Ying Shi, Gretik; Henry Erk, MEMC Electronics

Sunday, March 13

13:15-13:20
Chairman Remarks
David Huang   Praxair Electronics, USA

13:20-13:40
*Silicon and Wafer Technology Roadmap and Review (TBD)
Bing Dai   GCL Solar Energy Technology Holdings Limited, China

13:40-14:00
*Improvements on the Uniformities of a-Si/µ-Si Solar Thin Films and ECR Plasma Density Using Auxiliary Magnetic Field
Tomi Li   National Central University, Taiwan

14:00-14:20
*Hydrogenated Silicon Thin Film and Solar Cell Prepared by Electron Cyclotron Resonance Chemical Vapor Deposition Method
Jing-Yang Zhang, Yi-Ho Chu, Ching-Min Lin, Chien-Chia Lee, I-Chen Chen, Tomi Li
National Central University, Taiwan

14:20-14:40
*Amorphous Silicon Solar Module Reliability
Renhe Jia   Applied Materials Inc. US

14:40-15:05
Modeling and Characterization of Large-area Thin-film Modules for Performance and Yield Improvement on Production Line
Dapeng Wang   Applied Materials Inc. China

15:05-15:10
Research on Haze Control of ZnO Front Contact in Industrial Manufacturing
Cao Yu*, Baiheng Xu, Xinwei Niu, Tongyi Hao, Jingming Li, Liyou Yang
Chin Solar Technology, Zhejiang, China

Monday, March 14

Session II-I: Crystal Growth and Impurity Control
Session chairs: Deren Yang, Zhejiang University; Qi Wang, NREL

8:30-8:45
Analysis of Elemental Impurities in Trichlorosilane by Inductively Coupled Plasma Mass Spectrometry
Jiarong Chen   PerkinElmer, Inc.

8:45-9:00
Defect Evaluation by Photoluminescence for Uniaxially Strained Si and Strained Si-on-insulator
Dong Wang, Keisuke Yamamoto, Hongyi Gao, Haigui Yang, Hiroshi Nakashima
Kyushu University, Japan

9:00-9:15
Effects of the Transverse Magnetic Field on the Turbulent Fluctuations in the Melt of the Cz-Si Crystal Growth
Xin Liu*, Lijian Liu**, Yuan Wang
1. Xi’an Jiaotong University; 2. Zhejiang University

Session III: Device and Applications
Session chairs: Jenq-yang Cheng, National Central University; Tim Bao, BTU International

9:15-9:35
*Light Tripping for Efficient Crystalline Si Heterojunction Solar Cells
Qi Wang   NREL

9:35-9:55
*Increasing the Efficiency of Si-based Solar Cell Using Rare Earth Organic Complexes as Down-shifters
Simiona Binielli   University of Milano-Bicocca

9:55-10:15
Coffee Break

** Keynote  * Invited
**Session IV: Keynote Session - 1**

Session chairs: Renhe Jia, Applied Materials US; Qi Wang, NREL US

13:15-13:40
**Silicon Materials and Wafer Solutions for Electronic and Solar Industry (TBD)**
Tore Torvund, REC Silicon, President & CEO

13:40-14:05
**Multiphase Phenomena in Upstream Solar Silicon Processing**
Milind Kakani, MEMC, VP

14:05-14:30
**Solar Silicon Technology and Chinese Solar Industry (TBD)**
John R (Russ) Hamilton, GCL Solar Energy Technology Holdings Limited, CTO/VP

14:30-14:55
**Thin Film Silicon Technology for Building Integrated Photovoltaic (BIPV)**
Jeffrey Yang, United Solar Ovonic LLC, VP

14:55-15:10
Coffee Break

**Session V: Keynote Session - 2**

Session chairs: Renhe Jia, Applied Materials US; Qi Wang, NREL US

15:10-15:35
**Silicon Wafer Market: Outlook and Trends**
Dan Tracy, SEMI

15:35-16:00
**High Efficiency CIGS Film Solar Cell Technology**
Rommel Noufi, NREL, USA

**Session VI: Panel Discussion**

Moderator: David Huang, Praxair Electronics, USA

16:00-17:30
**Solar Silicon Material - Opportunity and Challenge**
Panelists: JA Solar, China
GCL Solar Energy, China
REC Silicon, USA
Wacker Chemie, Germany