Conference Agenda

PLENARY SESSION

Distinguished Conference Keynote Speakers

Dr. Peng Bai

CEO
Rong Semiconductor, China

Prof. John Robertson

Emeritus Professor of Electronic Engineering, Cambridge University, UK

Dr. Michael Chudzik

VP of Technology, IMS ICAPS &Packaging, Applied Materials, US

Prof. Tobias Delbruck

Professor in Neuromorphic Engineering, Institute of Neuroinformatics, Switzerland

Dr. Giorgio Allegato

MEMS Technology R&D Director, MEMS and Sensor Group, STMicroelectronics, Italy

Sunday, March 17, 2024
Meeting Room: 3rd Floor Auditorium

08:15-08:45 **Registration**

08:45-09:15 **Opening Ceremony**
Opening Remarks by Conference Chair
Opening Remarks by SEMI
Presentation of the Best Student Paper Awards and the Best Young Engineer Paper Awards

09:15-09:50 **Evolution of Moore's Law: a Perspective**
Dr. Peng Bai
CEO, Rong Semiconductor, China

09:50-10:25 **New Materials vs New Geometries in Electronic Devices**
Prof. John Robertson
Emeritus Professor of Electronic Engineering, Cambridge University, UK

10:25–11:00 **Integrated Module Approach to Solutions in the Specialty Device Market**
Dr. Michael Chudzik
VP of Technology, IMS ICAPS & Packaging, Applied Materials, USA

11:00–11:35 **50 Years of Silicon Retina History**
Prof. Tobias Delbruck
Professor in Neuromorphic Engineering, Institute of Neuroinformatics, Switzerland

11:35–12:10 **MEMS - Sustainable Technologies for a Sustainable World**
Dr. Giorgio Allegato
MEMS Technology R&D Director, MEMS and Sensor Group, STMicroelectronics, Italy

Panel Discussion
Sunday, March 17, 2024
Meeting Room: 3rd Floor Yellow River Hall

17:05-18:15 **AI for IC Design & Manufacturing: The Hopes, Challenges, and Opportunities**

Moderator: Prof. Cheng Zhuo, Zhejiang University

Panelists: Prof. Daniele Ielmini, Politecnico Di Milano;
Prof. Yu Wang, Tsinghua University;
Mr. Zusheng Yang, Empyrean
Dr. Jun Yuan, Qualcomm;
Prof. Runsheng Wang, Peking University;

Symposium I: Device Engineering and Memory Technology

Sunday, March 17, 2024 Shanghai International Convention Center
Meeting Room: 3rd Floor Yellow River Hall

Session I: In-memory Computing I
Session Chair: Hao Cai

***13:30-13:55**	**Implementation of Spintronic MRAM Circuits and Systems** Hao Cai, Southeast University
***13:55-14:20**	**Defect tolerant physics-inspired computing in memristor arrays** Can Li, University of Hong Kong
14:20-14:35	**Multifunctional RRAM Chip with Configurability for Sparsity-aware In-memory Isng Machine** Wenshuo Yue, Peking University
14:35-14:50	**A method of scalable polysilicon resistor by adjusting shielding metal in CMOS process** Hunjin Lee, X-FAB
14:50-15:05	**A 110nm BCD-on-SOI Technology offering Best-In-Class Nonvolatile Memory IP for Automotive Application** Boon Jiew Chee, X-FAB Sarawak Sdn. Bhd.
15:05-15:20	**Coffee Break**

Session II: In-memory Computing II
Session Chair: Xin Si

***15:20-15:45**	**2D devices and in-sensor computing** Feng Miao, Nanjing University
***15:45-16:10**	**SRAM based Compute-in-Memory Circuits Design for CNN and Transformers** Xin Si, Southeast University
***16:10-16:35**	**All-dielectric metasurfaces for vortex generation and Detection** Shumin Xiao, Harbin Institute of Technology
16:35-16:50	**Analog Device Engineering and Enhancement in 0.18um BCD on SOI Technology Platform** Poh Ching Sim, X-FAB Sarawak Sdn. Bhd.
16:50-17:05	**Innovative Test Solution Design and Production Practices for Automotive Based on ADVANTEST 93K** Jibao Fan, Advantest (China) Co., Ltd.

Monday, March 18, 2024 Shanghai International Convention Center
Meeting Room: 3rd Floor Yellow River Hall

Session III: Emerging Computing Technologies
Session Chair: Hao Wang

***08:30-08:55**	**2D Material Devices for Advanced Computing** Han Wang, University of Hong Kong
***08:55-09:20**	**A Full Spectrum of Computing-In-Memory Technologies** Zhong Sun, Peking University
09:20-09:35	**Inflection Points in CFET Scaling: Impact of DTCO Boosters** Dmitry Yakimets, Huawei Technologies R&D Belgium
09:35-09:50	**Ultrathin TiO_2 channel HfLaO FeFET with Low Operation Voltage** Xujin Song, Peking University

09:50-10:05 **Coffee Break**

Session IV: Memory Devices I
Session Chair: Jianshi Tang

***10:05-10:30** **Enhance Chip Connectivity and Functionality through RRAM-based Monolithic 3D Integration**
Jianshi Tang, Tsinghua University

***10:30-10:55** **Single Element Switch**
Min Zhu, Shanghai Institute of Microsystem and Information Technology

10:55-11:10 **First Principle Study on Oxygen Vacancy Induced Ferroelectricity in HfO_2-based ferroelectrics**
Chenxi Yu, Peking University

11:10-11:25 **Low Frequency Noise and Hot Carrier Degradation Characteristics on 55nm LP Platform**
Gang Wang, Hangzhou HFC Semiconductor Corporation

11:25-13:30 **Lunch Break**

Session V: Emerging Devices
Session Chair: Can Li

13:30-13:45 **A Novel Ultralow Voltage Slope Device**
Pengtao Li, Zhejiang University

13:45-14:00 **Experimental Investigation of Polarization Switching Speed in Ferroelectric HfO_2 for High-Speed and Low-Power Applications**
Hao Zheng, Peking University

14:00-14:15 **A Novel Hybrid-Channel Gate-All-Around Nanosheet Transistor For Leakage Control And Subthreshold Slope Reduction**
Yumin Xu, Fudan University

14:15-14:30 **Investigation of Self-Heating Effect on Forksheet Field-Effect Transistors**
Pan Zhao, Peking University

14:30-14:45 **Coffee Break**

Session VI: Memory Devices II
Session Chair: Kechao Tang

***14:45-15:10** **High endurance field-effect transistor memory based on Hafnium-oxide ferroelectrics**
Kechao Tang, Peking University

15:10-15:25 **Interface Treatment of Epitaxial Si FinFET Channel in Replace Metal Gate with Simultaneously Performance Improvement and Leakage Reduction**
Renjie Jiang, Institute of Microelectronics of the Chinese Academy of Sciences

15:25-15:40 **Experimental Investigation on the Back Gate Modulation of Extra-Thin Body pMOSFETs**
Rui Su, Zhejiang University

15:40-15:55 **Impact Of Thickness Dependent Ferroelectric And Interface Charge Variation On Device-To-Device Variation In Ferroelectric FET**
Fan Zhang, Xidian University/ IMECAS

Poster Session:

Yield Improvement in 4X Node Technology ETOX NOR-flash by Optimizing Control Gate Related Process and Design
Yihang Du, Huahong Semiconductor (WUXI) Limited

Machine Learning-based Performance Prediction Model Optimization for SOI LDMOS Using Adaptive Small Space Dataset

Jinwen You, Nanjing University of Posts and Telecommunications

HBM Device Test & Repair Solution on T5833

Xiang Ling, Advantest (China) Co., Ltd.

SUBSTRATE CURRENT IMPROVEMENT AND INVESTIGATION IN LOW VOLTAGE POWER LDMOS WITH A NOVEL DESIGN

Zhaozhao Xu, Huahong Semiconductor (Wuxi) Limited

Short-Loop Method to Shorten Gate Process Characterization Cycle Time

Bing Li, HangZhou HFC Semiconductor Corp.

Enhancement of SRAM Read and Write Noise Margin by Device Performance Adjustment

Ailin Li, Semiconductor Manufacturing North China (Beijing) Corporation (SMNC)

FABRICATION PROCESS IMPROVEMENT OF AGGRESSIVELY SCALED DUAL-BIT/CELL SPLIT-GATE FLOATING-GATE FLASH CELL

Yintong Zhang, Huahong Semiconductor (Wuxi) Limited

STI Gap-Filling Performance Improvement by the Process Integration Optimization in the 4Xnm ETOX Nor Flash

Zhuangzhuang Wang, Hua Hong Semiconductor (Wuxi) Limited

Breakdown Voltage Improvement of LDMOS by CESL Optimization in High-Voltage 90 nm BCD Technology

Ye Tian, Huahong Semiconductor (Wuxi) Limited

Research on the substitution of MIM capacitors and MOM capacitors on power devices

Wenwu Zhu, Huahong Semiconductor(Wuxi)

STUDY ON DNW PERFORMANCE IN 55NM CMOS

HAOQI ZHENG, Semiconductor Manufacturing International Corporation

STUDY ON NIPT SALICIDE WITH VARIOUS PLATINUM PERCENTAGE PERFORMANCE

HAOQI ZHENG, Semiconductor Manufacturing International Corporation

Anomalous Hot carrier injection induced degradation of drain current in HVMOS with STI

Bocheng Zhao, Shanghai University

Study of Improvement for substrate current in High-Voltage NMOS with Shallow Trench Isolation

Bocheng Zhao, Shanghai University

The Effect of Depth, Air Gap Width and Ion Implant on Deep Trench Isolation for BCD Technology

Chen Chen, Huahong Wuxi Semiconductor Manufactory Co., Ltd.

A new method for improving 8V ESD performance

Chuang Wang, Shanghai Huali Microelectronics Corporation

Fabrication of Semi-enclosed Control Gate of Semi-Floating Gate Transistor

Shiling Yang, Shanghai Huali Integrated Circuit Corporation

Threshold Voltage Mismatch Dependence of SRAM Yield Window Simulation

Chun-Hsiung Wang, HFC Semiconductor

Optimization of the 8T SRAM bitcell design

Lu-Ping Wu, HFC Semiconductor

SRAM Device Threshold Voltage Mismatch Investigation and Improvement

Chun-Hsiung Wang, HFC Semiconductor

Effect of lightly doped drain doping on variability for static random-access memory

Qiao Teng, Zhejiang University

Improvement of NLDMOS Performance in Low-Resistivity Substrate for Integration with Discrete Power Devices on One Chip

Yuncong Chen, HuaHong Grace Semiconductor Manufacturing Corporation

A photoelectric memristive devices for Artificial visual perception

Xuemeng Fan, Zhejiang University

Al_2O_3/AlOx Memristor with Nearly Ideal Synaptic Characteristics

Qian He, Zhejiang University

Two-Dimensional MoS_2 Based Memristors For Artificial Neural Network

Hailiang Wang, Zhejiang University

A Novel RRAM-Based TCAM Search Array

Zhen Wang, Zhejiang University

Static leakage failure analysis and improvement for small size SRAM

Minghui Zhu, Shanghai Huali Microelectronics Corporation

The Modeling and optimization of the Polysilicon Gate Line Width Roughness for Improving the Performance of 55nm CMOS devices

Yaoting Wang, Zhejiang University

Hot-Carrier-Induced Degradations and Optimizations for Lateral DMOS Transistor with Shallow Trench Isolation and Step Oxide Improvement

Zhibo Liu, Huahong Wuxi Semiconductor Manufactory

Virtual Fab Semiconductor Process Modeling Augmented Vertical Gate All Around Complementary FET based 6T SRAM path-finding

Zhaohai Di, Institute of Microelectronics, Chinese Academy of Sciences

Novel Memtransistor-based LIF Neuron with Tunable Ionic Dynamics for Spiking Neural Networks

Zhen Yang, Peking University

Ultra-low operating voltage RRAM devices regulated by nitride insertion layers

Zijian Wang, Zhejiang university

New Insight into Impacts from Read Cycle Number and Voltage Sweeping Direction on Memory Window of Ferroelectric FET

Chang Su, Peking University

IGZO-Ta2O5 Dual-layer CBRRAM: A Low Voltage and High Switching Ratio Storage Solution

Shengpeng Xing, Zhejiang University

The Optimization of the specific on-resistance of the VDMOS on the integrated platform of VDMOS and LDMOS

Xiaoqing Cai, HuaHong Grace Semiconductor Manufacturing Corporation

A STUDY OF PARASITIC CAPACITANCE SIMULATION IN DRAM BY VIRTUAL FABRICATION

Dempsey Deng, Lam Research

Benefits of Applied VSE High Current Implanters for White Pixel Reduction in Image Sensors

Shasha Wang, Applied Materials

Leakage Reduction Evolution With Gate Oxide Scaling

Yongchun Xuan, Applied Materials

Cost Effective Low Temperature Annealing Achieved by Producer Pyra

Yang Liu, Applied Materials

Advanced Ion Implanter with Metal Reduction Kit (MRK) for CIS White Pixel Improvement

Kui Shi, Applied Materials

Device performance (leakage & Rc) improvement by Trident XP CrionTM

Yuhang Jin, Applied Materials

Effective Tuning Knobs for High Current Implant Uniformity Optimization

Jinsong Lin, Applied Materials

Trident N/C co-implant for LDD dopant diffusion control

Zuoliang Han, Applied Materials

Solution-Processed Organic CMOS Inverter Via Contact Modulation

Jiarong Cao, Nanjing University of Posts and Telecommunications

Ultra-Short Channel Polymer Transistors

Zhiqi Xu, Nanjing University of Posts and Telecommunications

Exploring Low-Frequency Noise Behavior in Vertically Structured Organic Schottky Photodiodes

Tingting Ji, Nanjing University of Posts and Telecommunications

Flexible Low-Voltage, Hysteresis-Free Ferroelectric Polymer Transistors

Yao Yu, Nanjing University of Posts and Telecommunications

A comprehensive solution to parse, compare, convert, and compile TST pattern

Weilong Li, Teradyne

A Novel Approach for Doping Two-Dimensional MoS_2 Materials: ZnO Polar Interfacial Charge Transfer Method

Lijun Xu, Institute for Microelectronics, Chinese Academy of Science

Calculation Method of Target Erosion in the Planar DC Magnetron Sputtering

Jihua Ding, Beijing NAURA Microelectronics Equipment Co., Ltd.

Symposium II: Lithography and Patterning

Sunday, March 17, 2024 Shanghai International Convention Center
Meeting Room: 3H+3I+3J

Session I: Lithograpy/Etch joint session (II & III)
Session Chairs: Leo Pang / Ying Zhang

13:30-13:35 **Opening Remarks**

****13:35-14:05** **How Process, Equipment, Material, Computation that work together to make up the Performance of Photolithography**
Qiang Wu, Fudan University

****14:05-14:35** **Novel Etch Solution with Sym3 for Logic BEOL Patterning Etch Applications**
Hui Sun, Applied Materials

****14:35-15:05** **New Materials and New Functionalities Co-work scaling, and the Exploration of Inner Spacer Technique**
David Xiao, Qianmo Micros Design LLC

15:05-15:20 **Coffee Break**

Session II: Developments in Lithography
Session Chairs: Qiang Wu / George Lu

***15:20-15:45** **Recent progress of EUV Chemically Amplified Resist with Negative-Tone Development (CAR-NTD) for improving Chemical Stochastic**
Toru Fujimori, FUJIFILM Corporation

***15:45-16:10** **Acid Generation Efficiency Prediction by Bond Cleavage Calculation of EUV Photoacid Generators**
Jayoung Koo, DuPont

***16:10-16:35** **High-efficient nanofocusing for nanopattern with a plasmonic BNA**
Dandan Han, University of Chinese Academy of Sciences

Monday, March 18, 2024 Shanghai International Convention Center
Meeting Room: 3H+3I+3J

Session III: Process, Equipment, and Materials I
Session Chairs: Weiming Gao / Xiaoming Ma

****08:30-09:00** **From Tape to Mirrors: 50 Years of Progress in Photomask Technology**
Chris Progler, Photronics

***09:00-09:25** **The Influence of Aberration on 193 Nm Immersion (193i) Lithography Process Window**
Yanli Li, Fudan University

***09:25-09:50** **Polyimides for Power Device Applications**
Masao Tomikawa, Toray Industries Inc.

09:50-10:05

10:05-10:20 **Coffee Break**

Session IV: Computational Lithography
Session Chairs: Yayi Wei / Shiyuan Liu

***10:20-10:45** **Inverse lithography with adaptive mask complexity**
Xiaoxuan Liu, Guangdong University of Technology

10:45-11:10

***11:10-11:35** **Mask Corner Rounding in OPC Modeling**
Weimei Xie, National Integrated Circuit Innovation Center

11:35-11:50 **A Study of the Via Pattern Lithography Process Window under the 7 nm Logic Design Rules with 193 nm Immersion Lithography**
Jinhao Zhu, Fudan University

11:50-13:30 **Lunch Break**

Session V: Next DTCO and Design Optimization
Session Chairs: David Wei / Wenzhan Zhou

***13:30-13:55** **A Study of Flexible BEOL Design Rules Allowing Degreed Slanted Interconnection in Advanced Nodes**
Xianhe Liu, Fudan University

***13:55-14:20** **Research on Cross-Level Interconnection of Metal Layers under 193 Immersion Lithography Conditions**
Ying Li, National Integrated Circuit Innovation Center

***14:20-14:45** **A Study of the Minimum Area Rule under the 193 nm Immersion Lithography for Via and Cut Patterns**
Qiang Wu, Fudan University

14:45-15:00 **Coffee Break**

Session VI: Process, Equipment, and Materials II
Session Chairs: Wenzhan Zhou / Weiming Gao

***15:00-15:25** **The Spin-on Multi-Layer Material Status for Advanced Device**
Satoshi Dei, JSR Electronic Materials (Shanghai)

15:25-15:50

***15:50-16:15** **Enhancing High-throughput and High-precision CD-SEM Metrology Through Advanced Deep Learning-Based Image Processing**
Bo Wang, Hitachi High-Tech Corporation

16:15-16:30 **Correlation Between CD/LWR and Focus Level Fitting Error: A Process Quality Indicator**
Tianhao Huang, Zhejiang University

16:30-16:45 **The Impact of Wafer Warpage-Induced Unevenness on Alignment**
Pan Liu, Zhejiang University

Poster Session:

Pattern top loss improvement to enlarge process window for advanced node
Le Kuai, Nexchip Semiconductor Corporation

Coherence characterization for CDU budget breakdown in advanced DUV lithography
Wei Zhao, University of Chinese Academy of Sciences

Innovated Methodology Improving CD Uniformity for Lithography Using Wafer-less Dynamic Grouping Process Characteristics
Yong-Qiang Che, Semiconductor Manufacturing Beijing Corporation

Symposium III: Dry &Wet Etch and Cleaning

Sunday, March 17, 2024 Shanghai International Convention Center

Session I: Lithograpy/Etch joint session (II & III)
Meeting Room: 3H+3I+3J
Session Chairs: Leo Pang / Ying Zhang

13:30-13:35	**Opening Remarks**
****13:35-14:05**	**How Process, Equipment, Material, Computation that work together to make up the Performance of Photolithography** Qiang Wu, Fudan University
****14:05-14:35**	**Novel Etch Solution with Sym3 for Logic BEOL Patterning Etch Applications** Hui Sun, Applied Materials
***14:35-15:05**	**New Materials and New Functionalities Co-work scaling, and the Exploration of Inner Spacer Technique** David Xiao, Qianmo Micros Design LLC
15:05-15:20	**Coffee Break**

Session II: Advanced Patterning
Meeting Room: 3C+3D
Session Chair: Qingjun Zhao

***15:20-15:50**	**The New Developments in Etching of Dielectrics** Yuanwei Lin, Beijing NAURA Microelectronics Equipment Co., Ltd.
15:50-16:05	**Study of tungsten-doped carbon hard mask etch using O_2/NF_3 based chemistry** Li-Tian Xu, Beijing NAURA Microelectronics Equipment Co., Ltd.
16:05-16:20	**Plasma Corrosion Resistant ALD Coatings for Semiconductor Manufacturing Process Equipment** Lassi Leppilahti, Beneq
16:20-16:35	**A Study on SADP Film Stack Selection for Line Roughness Improvement in Planar 1xnm NAND Flash** Yinan Ma, Semiconductor Manufacturing North China (Beijing) Corporation
16:35-16:50	**A STUDY OF WAFER-LESS AUTO CLEAN EFFICIENCY PROMOTION METHOD IN DOUBLE PATTERNING DIELECTRIC HARD MASK PROCESS** Xinruo Su, Semiconductor Manufacturing North China
16:50-17:05	**Advanced Patterning Solutions for Logic and Memory Device Manufacturing** Taiyen Peng, Jiangsu Leuven Instruments Co., Ltd.

Monday, March 18, 2024 Shanghai International Convention Center
Meeting Room: 3C+3D

Session III: FEOL/MOL Etching
Session Chair: Hai Cong

08:45-09:00	**Challenge of boron-doped silicon hardmask etching** Xuehua Wang, Beijing NAURA Microelectronics Equipment Co., Ltd.
09:00-09:15	**Precise etching technology of ultra thin Al_2O_3 film using BCl_3 chemistry** Cheng Tian, Beijing NAURA Microelectronics Equipment Co., Ltd.
09:15-09:30	**Reactive Ion Beam Etching of Slanted Gratings for AR Applications** Shuo Dong, Jiangsu Leuven Instruments Co.Ltd.

***09:30-10:00**	**New development of ICP etching for advanced patterning** Zhongwei Jiang, Beijing NAURA Microelectronics Equipment Co., Ltd.
10:00-10:15	**Coffee Break**

Session IV: Resists Etch/Wet Etch/Clean/MEMS
Session Chair: Hai Cong

***10:15-10:45**	**Review of Advanced Ion Beam Etch Technology: Asymmetrical and Directional Approach** Yuxin Yang, Jiangsu Leuven Instruments Co., Ltd.
***10:45-11:15**	**The challenges and new developments on TSV etch applications** Guorong Li, Beijing NAURA Microelectronics Equipment Co., Ltd.
11:15-11:30	**High aspect ratio carbon hardmask etch process for profile and LCDU control** Mengjiao Zhu, Beijing NAURA Microelectronics Equipment Co., Ltd.
11:30-11:45	**Line edge roughness reduction in high aspect ratio carbon hardmask patterning for slit trench** Li Zeng, Beijing NAURA Microelectronics Equipment Co., Ltd.
11:45-12:00	**A Fully Automated VPD System for Noble Metal Control during CIS manufacturing** Qiao Huang, Jiangsu Leuven Instruments Co., Ltd.
12:00-13:30	**Lunch Break**

Session V: BEOL Etching and Memory Etch
Session Chair: Qingjun Zhao

***13:30-14:00**	**Challenges of Inductively Coupled Plasma Applications** Hu Zhou, Advanced Micro-Fabrication Equipment Inc. China
14:00-14:15	**Center to Edge Critical Dimension Uniformity Control in High Aspect Ratio Dielectric Etch** Jiayu Sun, Lam Research
14:15-14:30	**Profile Control for BEOL Tri-layer Patterning Scheme** Xingxing Xu, Lam Research
14:30-14:45	**Coffee Break**

Session VI: ALE and Patterning
Session Chair: Kaidong Xu

***14:45-15:15**	**Plasma etching solutions for compound semiconductors** Yali Fu, Beijing NAURA Microelectronics Equipment Co., Ltd.
15:15-15:30	**Perspective on Plasma Etching in Advanced Packaging** Yuanwei Lin, Beijing NAURA Microelectronics Equipment Co., Ltd.
15:30-15:45	**A Study on Floating Gate Profile Control and Reliability Improvement in Planar 1xnm NAND Flash** Jun Wang, Peking University
15:45-16:00	**Analysis of Key Factors in Reactive Ion Etching of SiC Gate Trench** Anton Kobelev, Suzhou STR Software Technology Co., Ltd.
16:00-16:15	**AlCu Residue Elimination Technique during BEOL Etch Process** Lian Ye, Jiangsu Leuven Instruments Co.Ltd.
16:15-16:30	**Ion Beam Etching as a Solution for Ultra-Precision Planarization Process** Lei Guo, Jiangsu Leuven Instruments Co., Ltd.
16:30-16:45	**Ultra low temperature high aspect ratio OX punch through etching** Hanlin Cui, Applied Materials

Poster Session:

An optimized approach for High-K first process reliability

Li Fei, Nexchip Semiconductor Corporation

An optimized process for high dielectric metal gate processes to avoid SiGe and NiSi contamination

Yongqiang Ding, HeFei JingHe Semiconductor Corporation

The LWR improvement in Metal hard mask etch

Songyu Liu, Nexchip Semiconductor Corporation

Metal line width roughness (LWR) improvement by different kind of photoresist (PR)

Chao Ding, Hefei Jinghe Semiconductor Corporation

Advanced Patterning LELE Cut LCDU Improvement

Ting Xie, Advanced Micro-Fabrication Equipment Company Inc.

Sidewall kink elimination of slanted gratings utilizing a twice-etching method

Jiuru Gao, Jiangsu Leuven Instruments Co., Ltd.

Residue Improvement in Liner OX Open Process

Ruxun Yuan, Lam Research

A STUDY ON THE DIFFERENT APPROACHS OF DUMMY GATE WET REMOVAL APPLICATION

Tianhao Zhang, Lam Research

Mandrel/Non-Mandrel Imbalance Improvement for Self-aligned Reverse Patterning Process

Shiming Zhang, Lam Research

Improvement of Outer Hole Profile Bending in High Aspect Ratio Dielectric Hole Etching

Taojun Zhuang, Lam Research

Improved Si Grass Control during Profile tuning for Silicon Trench Etch in Power MOSFET

Xi Chen, Lam Research

Profile Controlling in High Aspect Ratio Si Trench Etching by Steady-State-Process

Yaming Liu, Lam Research

Research of surface Particle contamination in Selective Nitride Etching Using hot Phosphoric Process

Sutao Liu, Nexchip Semiconductor Corporation

A study of TiN film queue time effect

Malong Cai, Nexchip Semiconductor Corporation

Ultra-Deep via Etching of Silicon Oxide for High-Voltage Capacitive Isolators

Yuyan Xia, Zhejiang University

Optimization of the Polysilicon Gate Etching Process in SONOS Memory Fabrication

Wanli Yang, Zhejiang University

A Study on Bevel Metal Film Remove for Bevel Peeling Defect Reduction

Liu Xuan, Semiconductor Manufacturing North China (Beijing) Corporation

Defect Improvement in Process Containing SiOx Passivation

JunMing Wang, Lam Research

Sn-Ag Compatible Selective Ti Etch in Cu RDL Fabrication and 3D IC Integration

Chien-Pin HSU, Avantor

Improvement of Line Roughness of Fin by Conventional Thermal Oxidation and Atomic Level Low-Temperature Ozone Treatments

Peng Wang, Integrated Circuit Advanced Process R&D Center Institute of Microelectronics of the Chinese Academy of Sciences

The Study of Buffer HF Solution Wet Etch Behavior in Trench Structure

Jiaming Shi, Grandit

Investigation of the Al Etching Rate Change in Copper Damascene Clean Formulation Chemical

Yipeng Wu, Grandit. tech.Co., Ltd.

Reaction temperature impact on Siconi® process

Songtao Lv, applied materials

MTBC Enhancement through new WET Clean implement for preventing wafer breakage

Chunlong Qiu, Applied Materials

A low-cost solution for Selectra™ Si Chamber Etch rate drift

Jing Cao, Applied Materials

Reduce AlF Byproduct Caused ESC Backside Helium Leak in Etch Chamber

Longjie Yu, Applied Materials

Impacts of Al_2O_3 Window aging on Plasma Ethcing Process

Yanfeng Zhao, Semiconductor Manufacturing International Corporation

TiN Hard Mask Open Comprehensive Study

Shuda Xu, Applied Materials

Improvement of CIS TM Profile by Adjusting Gas Ratio

Ziyue Xuan, Applied Materials

Al BEoL Via Etching Challenge and Solution on Producer-GT™

Sichao Zeng, Applied Materials

Producer-GT™ High Productivity CCP Etch Solution

Xipeng Tong, Applied Materials

Application of Advanced Pulsing Plasma on DRAM Buried Wordline Fin Profile and Micro Loading Control

Kevin Yao, Lam Research

Application of Hardware and Process Fine Tune for Chamber Matching in DRAM Critical Etch

Nick Fang, Lam Research

Buried-Worldline Omega-Shape Profile Control and Impact in DRAM

Liubo Ma, Lam Research

Mandrel Etch Tuning for Imbalance Improvement in Reverse SADP

Shipeng Gong, Lam Research

Inline Critical Dimension Uniformity Improvement in DRAM Capacitor Hard Mask Etch

Wei Wang, Lam Research

Bosch Process in TSV Application for Controllable Profile and Uniformity

Haoran Cao, Lam Research

Application of Advanced Pulsing and Novel Chemistry in DRAM Capacitor Etch Application

Haoran Cao, Lam Research

HAR HMO tilting offline monitor and chamber to chamber matching solution

Kai Hu, Applied Materials

Methods of Profile Control in HVCAP VIA Etching

Tongyao Zhao, Applied Materials

Profile Control of CIS BVia Silicon Etch
Le Jiang, Applied Materials
Control of BLC Trench Profile Angel in DRAM BLC Etch
Yuchen Jiang, Lam Research
Advanced Mixed Mode Pulsing in DRAM Active Area Etch
Zheng Ruan, Lam Research
The DRAM Capacitor LCDU Improved by Patterning Optimization
Yuyang Sun, Lam Research
A Study of Al etch process defects
Jiajie Li, Applied Materials
Advanced Pulsing in LELE Application for Controllable Profile
Hui Xu, Lam Research
300mm AL(0.5%Cu+1%Si) Etch Challenge and Solution on Advantage Edge Metal™
Jianjun Liao, Applied Materials
TiN selectivity improvement for All-in-one Etch
Yifeng Xu, Applied Materials
BCD process contact-etch challenges and solutions at Producer GT
Gang Sheng, Applied Materials
Filled Metal height uniformity optimization in BCAT
Lin Luo, Applied Materials
Study of A-Si as Dry Etch Hard Mask in BEOL Low-k Dielectric Patterning
Juxin Yin, Zhejiang University
Si Trench Profile Control in PMOS Silicon Recess Etching
Zhe Li, Lam Research
Study on Integrated Trench Etching for Trench-Type Power MOSFET
Jingru Shen, Zhejiang University
An approach to achieve a flat bottom in Si trench with oxide & poly pillar
Wei Gu, Applied Materials
Approaches of Pitch Walking Improvement in SAQP Patterning
Rishuai Zheng, Applied Materials
A Method of VIA Etch CD Range Improvement
Qunfeng Wen, Applied Materials
Effect of Low Damage Strip on Si and SiGe Surface State
Shijing Wang, Shanghai AnBang Semi Equipment Co., Ltd.
Oxide Remain Control for BCD ONO Spacer Etch on AMAT Producer GT_Wang Miao_Etch
Miao Wang, Applied Materials
Sym3 Chamber RF Plasma Stability Improvement
Jie Wang, Applied Materials
Gate oxide removal development for legacy node on SiCoNi
Fan Zhou, Applied Materials
Excellent Profile Control for Micro-OLED Anode Etch
Lijun Shan, Applied Materials
The influence of etching conditions on local loading in Deep Silicon Etching
Yiming Ma, Beijing NAURA Microelectronics Equipment Co., Ltd.

A STUDY OF DEEP HOLE ETCHING IN MO&DIELECTRIC ALTERNING MULTILAYER STRUCTURE

Zhe Wang, Beijing NAURA Microelectronics Equipment Co., Ltd.

A Study of High Aspect Ratio Si Trench in Cycle Mode Etching with Mask no Loss

Teng Zhang, Beijing NAURA Microelectronics Equipment Co., Ltd.

Side-wall angle uniformity improvement during ICP etch

Dong Li, Beijing NAURA Microelectronics Equipment Co., Ltd.

Two Step Etching Method for Removing Thick Photoresist

Long Ji, Beijing NAURA Microelectronics Equipment Co., Ltd.

Flattening the Silicon Nitride surface of semiconductor chips through etching

Donghan Wang, Beijing NAURA Microelectronics Equipment Co., Ltd.

Reducing Side Cutting During Wet Etching of Gate oxide layer for 28HK metal gate process

Chunshan Zhao, Shanghai Huali Integrated Circuit Corporation

A dry etch method to improve trench type oxide contact etch sidewall striation caused by incoming photo resist roughness

Shanshan (Sera) Nie, Lam Research

A Study on RCA clean particle performance improvement

Xiaowei Cheng, Lam Research

Application of Advanced Plasma Pulsing in a R-SADP (Reversed Self-aligned Double Patterning) Etch Process

Peng Zuo, Lam Research

Novel Method for Titanium Nitride Wet Etch Thickness Dynamic Control

Chen Zhang, Lam Research

Wafer Thinning Thickness Control with In-situ Measurement on Rough Silicon Surface

Zhi Shen, Lam Research

Nested Bosch Process

Changhuo Liu, Semiconductor Manufacturing North China

Optimized AMMP for High Aspect-Ratio Bottom Contact Open Process in DRAM Applications

Rick Yang, Lam Research

Symposium IV: Thin Film, Plating and Process Integration

Sunday, March 17, 2024 Shanghai International Convention Center
Meeting Room: 5th Floor Yangtze River Hall

Session I: Device Integration - 1
Session Chair: Xiaoping Shi

13:30-13:35	**Opening Remarks**
***13:35-14:00**	**Tailoring the deposition and composition of advanced oxide and SiCN films to deliver the highest bonding energy for fusion and hybrid bonding applications** Zongbin Wang, Applied Materials
***14:00-14:25**	**A Review in III-Nitride Nanocolumns Growth and Applications** Enrique Calleja, Universidad Politécnica de Madrid
***14:25-14:50**	**Advances and Reliability Challenges in Heterogeneous Integration in Chiplet Era: from Solder to Copper to Optical Interconnects** Zhuo-Jie Wu, HFC Semiconductor
14:50-15:10	**Optimization of Deep Trench Isolation on 0.18μm SOI BCD Technology for Automotive Application** Siti Aisah Mohd Salleh, X-FAB Sarawak Sdn. Bhd.
15:10-15:25	**Coffee Break**

Session II: Device Integration - 2
Session Chair: Chao Zhao

***15:25-15:50**	**The Progress and Challenges of Large Scale Integration of Silicon Photonics** Adam Lewis, CUMEC
***15:50-16:15**	**Do we need 300mm GaN?** Kai Cheng, Enkris Semiconductor,Inc
***16:15-16:40**	**Si based GaN HEMTs/System R&D and the perspective of the technological commercialization** Hongyu Yu, Southen University of Science & Technology

Monday, March 18, 2024 Shanghai International Convention Center
Meeting Room: 5th Floor Yangtze River Hall

Session III: ALD Process Development - 1
Session Chair: Jianhua Jv

***08:30-08:55**	**Thin Film Atomic Layer Deposition and Selective Processes** Rong Chen, Huazhong University of Science and Technology
***08:55-09:20**	**A Chemistry Perspective of ALD Precursors' Properties** Xiabing Lou, Origin Deposition Materials Co., Ltd.
09:20-09:40	**Characterizing low-k (SiCON) film with different element composition** Wenxu Duan, Beijing NAURA Microelectronics Equipment Co., Ltd.
09:40-10:00	**ALD of Dielectric Materials: Analysis of Equipment Design and Process Performance Using Detailed Modeling** Yanlin Mao, Suzhou STR Software Technology Co., Ltd.
10:00-10:20	**Coffee Break**

Session IV: Memory Technology
Session Chair: Jiaxiang Nie

***10:20-10:45**	**Design Technology Co-optimization for Yield and Reliability Enhancement of RRAM Technology Platform** Zhichao Lv, Reliance Memory
***10:45-11:10**	**The effect of stress on HfO_2-based ferroelectric thin films** Feng Luo, Nankai University
***11:10-11:35**	**SiGe/Si Heteroepitaxial Epitaxy and Characterization for CMOS and Vertically Stacked DRAM** Guilei Wang, Beijing Superstring Academy of Memory Technology
***11:35-12:00**	**Modeling of Endurance Degradation of Anti-ferroelectric $Hf_{1-x}Zr_xO_2$ Capacitor** Yaru Ding, Zhejiang University
12:00-13:30	**Lunch Break**

Session V: Device Integration - 3
Session Chair: Chenyu Wang

13:30-13:50	**The Formation of Air-gaps Isolation Used in Metal/Dielectric Stacking** Weidu Qin, Beijing Superstring Academy of Memory Technology
13:50-14:10	**SMT OPTIMIZATION OF PMOSFET BASED ON MULTI-DEPOSITION AND IN-SITU N2 PLASMA TREATMENT** Longyue Zheng, Zhejiang University
14:10-14:30	**FEA of Thermo-mechanically Induced Crack in IMD** Colin Chan, X-FAB Sarawak Sdn. Bhd.
14:30-14:50	**Backside Deposition of LTO/Poly-Si Sealing Layer by One-step PECVD and Post Annealing** Junxian Gao, Lam Research
14:50-15:10	**Copper Diffusion Improvement by Optimizing TaN and Integration in Power Device** Xiangyu Zhou, Beijing NAURA Microelectronics Equipment Co., Ltd.
15:10-15:30	**A machine learning study to obtain an optimal processing pulsed frequency on reactive pulsed DC sputtering of aluminum nitride films** Xue-Li Tseng, National Central University
15:30-15:45	**Coffee Break**

Session VI: Process Development - 1
Session Chair: Xun Gu

15:45-16:05	**Full Wafer Combinatorial Deposition with In-situ XPS/UPS Characterizations** Weimin Li, Shanghai Institute of IC Materials Co., Ltd.
16:05-16:25	**Tungsten Surface Roughness Improvement by Single Deposition Process** Zhengning Gao, Lam Research
16:25-16:45	**The Effects of Different Silicon Oxide Substrates on Amorphous Silicon Thin-Film** Zhengdao Liu, Beijing NAURA Microelectronics Equipment Co., Ltd.
16:45-17:05	**A Novel Thin Film Deposition Method by IBD for Asymmetrical Patterns** Zichao Li, Leuven Instruments
17:05-17:25	**Potential confusion in the analysis of the current-voltage characteristics of high-k dielectric on lightly doped p-type silicon MIS capacitors** Wai Shing Lau, Nanyang Technological University

17:25-17:45 **The secret of the leakage current mechanism in some historical device-quality high-k metal-insulator-metal capacitors**
Wai Shing Lau, Nanyang Technological University

Poster Session:

Optimizing Si/SiO_2 Interface of Planar LDMOS Field-Effect Transistors for Medium-Voltage Power Applications
Jiaoyang Chen, Huahong Semiconductor (Wuxi) Limited

Study of HDPCVD Charge Improvement for ILD Process
Jie Yang, Lam Researchc

IMPROVED PERFORMANCE OF PMOS BY OPTIMIZING THE EPITAXIAL MORPHOLOGY
Tao Wang, Shanghai Huali Integrated Circuit Corporation

Exploring the Effect of Gate Oxide Process on the Electrical Performance of the CMOS Device
Yongkang Hu, University of Science and Technology of China

Improving Gate Oxide Uniformity Using Wet-Dry Oxidation
Lin Tang, School of Micro-Nano Electronics, Zhejiang University

NiSix Anneal on Producer Pyra
Heping Du, Applied Materials

DRAM Bit line Evaluation by using Single Precursor Activate Radical Chemistry (SPARC) Process
Guanfeng Lu, Lam Research

W CVD Process Extendibility Development for Challenging Gap Fill
Shao Rui, Applied Materials

NBTI Improvement Through Gate Process Optimization
Ying Ma, Applied Material China

Excellent Performance of PC XT in Soft-Clean
Xingluan Long, Applied Materials

Amorphous Silicon Bump Defect Mechanism Analysis and Improvement Strategy
Shudi Min, Applied Materials

Approach of Customized Thickness Profile and Superior Uniformity on SACVD
Xiang Li, Applied Materials

HARP STI Wafer Sliding and Pre-heat Improvement by Recipe Optimization
Yiyu Zhang, Applied Materials

HARP STI Range Improvement for 28nm HKMG Double Patterning Process
Zhaojie Sun, Applied Materials

High Bow wafer Handling Approach on Producer PECVD
Bin Wang, Applied Materials

Low Dep Rate Oxide Process Development for Glue Layer
Congcong Zhao, Applied materials

Excellent Stability Control for High Throughput DARC Process
Chao Zheng, Applied Materials

N-Dosage Non-Uniformity Tuning in Nitride Incorporated Gate Oxide Process
Eira Yang, Applied Materials

High Productivity of Advanced Al PVD in Al Slab
Xiaogang Su, Applied Materials

SiGe Epitaxy Improved by Si Cap Technology

Tao Wang, Shanghai Huali Integrated Circuit Corporation

Effect of process parameters on microstructure and properties of ITO films by pulsed magnetron sputtering

Yanmeng Chen, Beijing NAURA Microelectronics Equipment Co., Ltd.

The Influence of Different Parameters on Capacitive Coupled Magnetron Sputtering Process

Song Yang, Beijing NAURA Microelectronics Equipment Co., Ltd.

Effect of process gas pipline on TiN film resistance

Hongwei Geng, Beijing NAURA Microelectronics Equipment Co., Ltd.

TiN Infilm Particle Improvement by Bias Field Integration

Xin Wang, Beijing NAURA Microelectronics Equipment Co., Ltd.

Tool transfer compatibility improvement for different thin wafer type

Jiaxi Liu, Applied Materials

Symposium V: CMP and Post CMP Cleaning

Sunday, March 17, 2024 Shanghai International Convention Center
Meeting Room: 5D+5E

Session I: prensent and future
Session Chair: Xinping Qu

****13:30-14:00**	**CMP equipments and application technologies for advanced manuafacturing process** Xinchun Lu, Tsinghua University
***14:00-14:25**	**CMP Technology for More than Moore Innovation** Haedo Jeong, Pusan National University
***14:25-14:50**	**New methodology for anisotropic nanoparticles characterization by polarization light scattering: length and diameter determination of rod-like nanoparticles** David Jacob, Cordouan Technology
14:50-15:10	**Coffee Break**

Session II: ILD and STI slurry
Session Chair: Shoutian Li

***15:10-15:35**	**Ceria slurry applications to STI, ILD and advanced packaging CMP** Yuchun Wang, Anji microelectronics
***15:35-16:00**	**From Good to Great: The Power of Advanced ILD CMP Slurries in Boosting Performance** Juliane Hitzel, Advanced NanoSurface Technologies Co., Ltd.
16:00-16:15	**CeO_2 slurry post rinse condition research in STI CMP technology** Zhengyi Li, Semiconductor Manufacturing North China (Beijing) Corp.
16:15-16:30	**INCOMING IMPACT ON DISHING IMPROVEMENT IN FEOL PROCESS** Huize Du, Shanghai Huali Integrated Circuit Corporation, Shanghai, China
16:30-16:45	**Positively charged ceria particles cleaning by HCOOH-H_2O_2-DIW solution** Wenlong Tang, Fudan University
16:45-17:00	**Study on the dispersing effect and mechanism of LABSA on SiO_2 in an alkaline barrier slurry** Fangyuan Wang, Hebei University of Technology

Monday, March 18, 2024 Shanghai International Convention Center
Meeting Room: 5D+5E

Session III: Metal CMP
Session Chair: Jingxun Fang

***09:00-09:25**	**Mechanism Research and Improvement of AL Scratch Defect Based on MG CMP** Qingqing Duan, Shanghai Huali Integrated Circuit Corp.
09:25-09:40	**Cu post CMP cleaner development utilizing AI system** Atsushi Mizutani, Fujifilm corporation
09:40-09:55	**Effect of Green Corrosion Inhibitors on the Performance of Copper-Cobalt CMP** Chao He, Institute of Microelectronics, Hebei University of Technology
09:55-10:10	**Effect of Green Additive Sarcosine as Inhibitor for Cobalt-Based Copper Interconnect CMP** ChangXin Dong, Hebei University of Technology
10:10-10:30	**Coffee Break**

Session IV: Compound Semiconductor CMP
Session Chair: Baoguo Zhang

***10:30-10:55**	**The development progress of new high-efficiency silicon carbide substrate polishing slurry** Xiuyan Sun, Zhangjiagang Anchu Technology Ltd.
***10:55-11:20**	**Research on the electro-fenton magnetorheological finishing technology for GAN wafer** Qiusheng Yan, Guangdong University of Technology
11:20-11:35	**Study on the Slurry for Chemical Mechanical Polishing of GaN Wafer** Steve Liu, Hebei University of Technology
11:35-13:30	**Lunch Break**

Session V: Novel Films CMP and Process
Session Chair: Jie Chen

***13:30-13:55**	**CMP characteristics of IGZO thin film with a variety of process parameters** Ming Zeng, Beijing Superstring Academy of Memory Technology, Beijing, China
***13:55-14:20**	**Study on the Processing Characteristics and Polishing Technology of Easily Cleavable Gallium Oxide Crystals** Hai Zhou, Yancheng Institute of Technology
14:20-14:35	**Chemical Effect Mechanism in Chemical Mechanical Polishing of Silicon Wafer** Chenwei Wang, Jiangsu Shanshui Semiconductor Technology Co., Ltd.
14:35-14:50	**EOE evolution processes of same step profile in CMP with different one-material polishing time** LIXiao Wu, Lanzhou University of Technology
14:50-15:05	**Effect of Surfactants on CMP Properties of C-, A- and R-plane Sapphire** Xinjie Li, Hebei University of Technology
15:05-15:25	**Coffee Break**

Poster Session:

A Novel Endpoint System Application On DRAM W CMP Application

Lin Wang, Applied Materials

DISHING STUDY ON CHEMICAL MECHANICAL PLANARIZATION (CMP)

Huize Du, Shanghai Huali Integrated Circuit Corporation, Shanghai, China

ILD-CMP Wafer Edge Thickness Profile Stability Improvement Via Acid Silicon Oxide Slurry Formulation Design

Zhijie Zhang Liang Tian, Semiconductor Manufacturing North China (Beijing) Corp, Beijing, China

Study on Ceria Slurry for Chemical Mechanical Polishing of 4H-SiC

Sihui Qin, Hebei University of Technology

The effect of CeO_2 / SiO_2 composite abrasive on the performance of silicon CMP under low concentration conditions

Liu Wenbo, Hebei University of Technology

Chemical Mechanical Planarization of SiC Si-face by Al2O3-based acid slurry

Zehao Yue, Hebei University of Technology

Multiple approaches to achieve high throughput of Cu CMP process in LK 3 platens platform

Jiaming Xu, Applied Materials

Achieved World-Class BSI Si CMP TTV Performance via FVXE NIR® MPC System

Likun Cheng, Applied Materials

Study on chemical-mechanical synergies in polishing of ruthenium
Hongyu Di, Dalian University of Technology
Effects of Polyvinyl Alcohol on Silicon Chemical Mechanical
Shuangshuang Lei, Hebei University of Technology
Motor torque algorithm and polish pressure optimization in STI CMP Process
Chen Qiang, Applied Materials
RTPC XE for 28nm BEOL Cu CMP
Youlai Xiang, Applied Materials (China), Inc. China
Study on 28nm Technology Node ILD0-CMP Micro_Scratch Defect Reduction
Xing Ma, Shanghai Huali Integrated Circuit Corp.
China 1st RTPC X/Fullscan X implemented in LK Metal CMP
Zhenxing Song, Applied Materials (China)
Feasibility Analysis of Skip ILD-CMP Scheme on 28nm Technology Node
Fan Chen, Shanghai Huali Integrated Circuit Corp.
A Trade-off Balance Between Cu Corrosion and Cu Oxide Defect
Chenyu Zhou, Shanghai Huali Integrated Circuit Corp.
The Precise Profile Control of RTPC X in CIS Cu CMP
Mengxia Li, Applied Materials
Micro-Scratch Defect Improvement for CMP Process
Kun Zhang, Applied Material

Symposium VI: Metrology, Reliability and Testing

Sunday, March 17, 2024 Shanghai International Convention Center
Meeting Room: 3B

Session I: Test I
Session Chair: Xiaowei Li

13:30-13:35	**Opening Remarks**
***13:35-14:00**	**Jitter reduction for multi-GHz ATE up to 20 GHz** Dave Keezer, Eastern Institute for Advanced Study (EIAS) in Ningbo, China.
***14:00-14:25**	**Assessing the Power-Awareness of VLSI Testing** Xiaoqing Wen, Kyushu Institute of Technology, Japan
14:25-14:40	**An Efficient Library for Protocol Test on V93000** Peifeng Ni, Advantest (China) Co., Ltd.
14:40-14:55	**Address the challenges of mass production testing for 5G millimeter devices** Daniel Sun, Advantest (China) Co., Ltd.
14:55-15:10	**Highly multi-sites front end test solution design and implementation for automotive testing** Kaitao Liu, Advantest (China) Co., Ltd.
15:10-15:25	**Mirroring ATPG Technology for Multi-Core Chips** Jitong Zhou, Sanechips Technology
15:25-15:40	**Deep Reinforcement Learning-Based Automatic Test Pattern Generation** Wenxing Li, Institute of Computing Technology, Chinese Academy of Sciences
15:40-15:55	**Coffee Break**

Session II: Metrology I
Session Chair:

***15:55-16:20**	**Doping level detection in Si or SiGe via In-Line Raman Spectroscopy** Ilya Osherov, Nova Ltd.
16:20-16:35	**Investigation on the root cause of ESD failure of large size WBBGA package chip** Yunhe Zhang, Sanechips Technology Co., Ltd.
16:35-16:50	**The Influence of Pin Position on CDM Peak Current of Chips Based on Large-Sized CoWos Package** Liyi He, Sanechips Technology Co., Ltd.
16:50-17:05	**Depth-profile Analysis of AlAsGa film via Grazing Incident X-ray fluorescence** Xujun Li, Shenzhen Angstrom Excellence Semiconductor Technology Co., Ltd.

Monday, March 18, 2024 Shanghai International Convention Center
Meeting Room: 3B

Session III: Test II
Session Chair:

***08:30-08:55**	**Polymorphic Circuits Design and Applications in Security** Gang Qu, University of Maryland, USA
08:55-09:10	**Breakthrough the test challenges for the latest Beidou navigation and satellite communications chips** Xi Liu, Advantest (China) Co., Ltd.

09:10-09:25	**Advanced Digital Baseband Signal Generation and Processing Solution for V93000 5G Small Cell Transceiver Testing** Bank Liu, Advantest (China) Co., Ltd.
09:25-09:40	**Various Driver test Summary on V93000 in Automotive Device** Yang Lin, Advantest (China) Co., Ltd.
09:40-09:55	**A new fast XRD apparatus for the epitaxial films with a focusing X-ray Beam** Yankun Sun, Shenzhen Angstrom Excellence Semiconductor Technology Co., Ltd.
09:55-10:10	**An Efficient Protocol ATE Solution for Driver IC on Advantest T6391** Xiang Cai, Advantest (China) Co., Ltd.

Session IV: Metrology II
Session Chair:

***10:10-10:35**	**MI's solutions for next era** Byoung-Ho Lee, Hitachi High-Tech Corporation
10:35-10:50	**Metryx solution for dishing defect in Ultra thick metal ECP process** Joey Hu, Lam Research
10:50-11:05	**Assessing Brittleness of Substrates and Thin Layers with Nanoindentation** Zhiming Zhang, KLA Instruments Group
11:05-11:20	**Advantages of Picosecond Laser Acoustics to Process Control of Semiconductor Power Devices** Johnny Dai, Onto Innovation
11:20-11:35	**Multi-physics Simulation of Electromigration in Cu Interconnect** Xuefeng Zhang, Beijing NAURA Microelectronics Equipment Co., Ltd.
11:35-11:50	**Analysis and Protection Solution for Aging DC-stress Induced Waveform Distortion Issues** Haiyong Wang, Sanechips Technology Co., Ltd.
11:50-12:05	**Modern X/Y metrology system addressable to mature semiconductor nodes** Xueying Hai, Mycronic AB
12:05-13:30	**Lunch Break**

Session V: Reliability
Session Chair:

***13:30-13:55**	**Signal and Power Reliability for Integrated Chips and Chiplets** Lei He, UCLA, USA
13:55-14:10	**Electro Optical Time Domain Reflectometry for Advanced Package Failure Analysis** Longhai Liu, Advantest (China) Co., Ltd.
14:10-14:25	**Test solution to prevent Dynamic Voltage Stress burning issue on ATE** Haijing Wu, Advantest (China) Co., Ltd.
14:25-14:40	**Reliability challenges in SiC components – performing dynamic test methodologies like DGS for meaningful measurement results** Sandro Strasser, SET GmbH, NI
14:40-14:55	**Study on Failure Mechanism of C4 Bump Solder Excursion in CoWoS Package** Xixiong Wei, Sanechips Technology CO., Ltd.
14:55-15:10	**Coffee Break**

Session VI: Test III
Session Chair:

***15:10-15:35**	**Scaling of Memory Performance and Capacity with Memory Processor** Fei Wang, Shandong University
15:35-15:50	**Novel Process Control Solutions for Advanced Power and Automotive Semiconductor Devices** Terry Chen, Applied Materials
15:50-16:05	**A Dynamic Reusable Structure of I/O Pads for Scan Chains** Qi Cheng, Sanechips Technology
16:05-16:20	**V93000 test solutions introduction for Audio PA device** Junlin Wang, Advantest (China) Co., Ltd.
16:20-16:35	**A Closed-loop Chip Fast Binning Technology** Jiawei Wang, Sanechips Technology

Poster Session:

Test solution of mini-LVDS interface transmitter for media chip on V93000 platform
Ying He, Advantest (China) Co., Ltd.

Testing implementation and challenges of processor with power path switching feature
Liuhao Chen, Advantest (China) Co., Ltd.

A fast measurement scheme for high-speed loopback pin continuity testing
Liuhao Chen, Advantest (China) Co., Ltd.

A New Flexible Binning Method in ATE Production
Hanru Zhang, Advantest (China) Co., Ltd.

A Universal DPAT GUI Solution for Production Test
Hao Chen, Advantest (China) Co., Ltd.

Picosecond Ultrasonics Applications on Electroplated Cu Process
HuaYuan Li, Onto Innovation

A Robust Calibration Test Solution for High-Performance Computing SoC Tsensors
Yang Zhang, Advantest (China) Co., Ltd.

A common framework solution for firmware test on V93000 ATE platform
Yanyan Chang, Advantest (China) Co., Ltd.

Study of Coating Effect on TEM Sample Damage and Elemental Analysis
Yun Xu, SMIC

A Universal Auto Configured Efuse Solution on ADVANTEST V93000 ATE Platform
Yefang Wang, Advantest (China) Co., Ltd.

Optimized Filling Capacity in HARP Process for STI void Defect Improvement in 28nm Technology
Zhimin Zhang, Shanghai Huali Integrated Circuit Corporation

Influence of Foup Environment On Defects in Semiconductor manufacturing
Weiwei Zhao, Shanghai Huali Integrated Circuit Corporation

Streamlining Chip Testing with Simplified Digital Data Acquisition
Felix Chen, Advantest (China) Co., Ltd.

Comparison of simulation and test results of multi-type ring oscillators on advanced process nodes
Kuili Chen, Sanechips Technology

Optimization and Validation of Sampling and TD-GCMS Analysis for Volatile Organic Compounds from Semiconductor Cleaning Coupons

Ling Wang, Ferrotec Technology Development (Shanghai) Co., Ltd.

Application of Pulse Id-Vg Technique on 55nm Low Power Platform

Gang WANG, Hangzhou HFC Semiconductor Corporation

New Generation Test Framework Solution for Complicated Multi-Die Chip on ATE

Kai Zhou, Alibaba-Thead

Virtual Measurement Combine OCD and FDC through Optimized Random Forest Machine Learning Algorithm Assists on Post Etching Monitor

Qingyun Yang, SiEn (Qingdao) Integrated Circuits Co., Ltd.

Characterization of Ultrathin Films in HKMG by Spectroscopic Ellipsometer

Yufan Zhang, Shenzhen Angstrom Excellence Semiconductor Technology Co., Ltd.

Study on STEM EDS for GeSi Atomic Layer Interface Identified and Concentration Quantified

Fan Zhang, SMIC

An optimized ADC&DAC test solution from SmartScale MCx to ExaScale WSMX

Tianyu Zhang, Advantest (China) Co., Ltd.

Spectra Machine Learning for the Prediction of Sheet Resistance and Capacity

Shang Li, SiEn (Qingdao) Integrated Circuits Co., Ltd.

Quantitative analysis of the damage degree of the single-crystal silicon induced by ion implantation using an optical approach

Emma Wu, SiEn (Qingdao) Semiconductor corporation Co., Ltd.

Detecting the B concentration in the SiGeB epilayers utilizing a hybrid approach combining HR-XRD and XPS

Emma Wu, SiEn (Qingdao) Semiconductor corporation Co., Ltd.

A new multi-mode X-ray fluorescence apparatus for both blanket and pattern wafer film metrology

Yuxiang Huang, Shenzhen Angstrom Excellence Technology Co., Ltd.

The Influence of Metal Barrier Punch Through Process on Dielectric Reliability at 55nm CMOS node

Chenxiao Xu, Zhejiang University

Tunability Demonstration of RadiancePlus® on Spike Anneal Process

Xiaolong Wang, Applied Materials

Sample Preparation Method for In-Situ Tem Analysis in Integrated Circuits

Guoyang Ye, Semiconductor Manufacturing International (Shanghai) Corporation Failure Analysis Laboratory

Symposium VII: Packaging and Assembly

Sunday, March 17, 2024 Shanghai International Convention Center
Meeting Room: 5B+5C

Session I: 3D and Advanced Packaging Technologies
Session Chair: Steve X. Liang

13:30-13:35	**Opening Remarks**
***13:35-14:00**	**Chiplets and Advanced Packaging for Future Computing** Terry Wu, Samsung Electronics
14:00-14:20	**Challenges of Semiconductor Micro Via Fabrication Technology for 3D Chiplet Interconnect** Yasuhiro Morikawa, ULVAC, Inc.
14:20-14:40	**Comprehensive Investigation of Insufficient IMC in SOIC Through Advanced Statistical Analysis** Jingwei Sun, NXP Semiconductors
****14:40-15:10**	**Heterogeneous Integration Ecosystem: The Critical Path to the Success of 3D SOC(SOH)** Eason Wang, ICLeague
15:10-15:30	**Coffee Break**

Session II: Novel Packaging Materials and Process
Session Chair:

15:30-15:50	**Hybrid Wafer-to-Wafer and Die-to-Wafer Technology for Heterogenous Integration Applications** Viorel Dragoi, EV Group
15:50-16:10	**Glass As An Enabling Material for Advanced Packaging** Jay Zhang, Corning Incorporated

Monday, March 18, 2024 Shanghai International Convention Center
Meeting Room: 5B+5C

Session III: Inspection, Test and Reliability
Session Chair: X. Wu

***09:00-09:25**	**Study on ELK Dielectric Reliability During the Solder Reflow Process Based on Finite Element Simulations** Jialin Zheng, Sanechips Technology Co., Ltd.
09:25-09:45	**A Modularized Thermal Test Chip Design and Verification** Jianjun Sun, Sanechips Technology Co., Ltd.
09:45-10:05	**Evaluating 224G SI Performance of Vertical Interconnections on Package Substrate and PCB** Kai Yuan, Sanechips Technology Co., Ltd.
10:05-10:20	**Coffee Break**

Session IV
Session Chair: M. Huang

10:20-10:40	**Heat Transfer Improvement of Phase Change Material with Metal Foam** Yan Zhang, Shanghai University

***10:40-11:05** **Study of Defects in Advanced Packing at the Atomistic Scale by Using In Situ TEM**

Xing Wu, East China Normal University

***11:05-11:30** **The Solution and Challenge of Glass Core Substrate Technology**

Tingyu Lin, Guangdong FoZhiXin (FZX) Microelectronics Technology Research Co., Ltd.

***11:30-11:55** **Breaking Memory Wall with SeDRAM® Technology in Chip Level**

Fengguo Zuo, Xi'an UniIC Semiconductors Co., Ltd.

Poster Session:

Thermal and Thermal Stress Simulation Analysis of Embedded Microchannel Cooling on Large-Size Packaging

Fusheng Meng, Sanechips Technology Co., Ltd.

Improvement of Warping Simulation Accuracy and Influence Factors Analysis in FCBGA Package

Yubo Wang, Sanechips Technology Co., Ltd.

Symposium VIII: MEMS, Sensors and Emerging Semiconductor Technologies

Sunday, March 17, 2024 Shanghai International Convention Center
Meeting Room: 5A

Session I: Emerging materials and devices
Session Chair: Jianshi Tang, Tsinghua University

13:30-13:35	**Opening Remarks**
***13:35-14:05**	**Advancing 3D Nano-electronic Systems through Innovations in BEOL-Compatible Oxide Semiconductor Technology** Gong Xiao, National University of Singapore, Singapore
***14:05-14:35**	**XOI materials** Xin Ou, Shanghai Institute of Microsystem and Information Technology, China
***14:35-15:05**	**Si based GeSn materials and devices** Chuanbo Li, Minzu University of China, China
15:05-15:20	**Coffee Break**
***15:20-15:50**	**Antimonide semiconductor material for infrared sensing** Donghai Wu, Institute of Semiconductors, China
***15:50-16:20**	**Lamb Acoustic Wave Device for RF applications: Ready for Prime Time Challenges and Applications?** Songbin Gong, Spectron Tech, C4hina/UIUC, USA

Monday, March 18, 2024 Shanghai International Convention Center
Meeting Room: 5A

Session II: 2D materials
Session Chair: Wei Wang, Peking University

08:30-08:35	**Opening Remarks**
***08:35-09:05**	**Controllable preparation of wafer-scale two-dimensional van der Waals heterostructures** Libo Gao, Nanjing University, China
***09:05-09:35**	**Atomically sharp interface of van der Waals heterostructures enabled high-performance electronic devices** Lihong Bao, Institute of Physics, Chinese Academy of Sciences
***09:35-10:05**	**NEMS based on novel vdW heterostrucutres** Zheng Han, Shanxi University, China
10:05-10:20	**Coffee Break**
***10:20-10:50**	**High-mobility 2D P-type semiconductor materials** Xiang Chen, Nanjing University of Science & Technology, China
***10:50-11:20**	**Universal Materials and Device Integration Technology for Future Chips** Chen Wang, Tsinghua University, China
11:20-11:40	**A Graphene Field Effect Transistor (GFET) based Integrated Biosensor System For Point-Of-Care Application** Ziyang Zhu, Fudan University, China
11:40-13:30	**Lunch Break**

Session III: MEMS & Sensors
Session Chair: Chen Wang, Tsinghua University

13:30-13:35 **Opening Remarks**

***13:35-14:05** **A GHz Silicon-based Width Extensional Mode MEMS Resonator with high Q**
Jinling Yang, Institute of Semiconductors, Chinese Academy of Sciences

***14:05-14:35** **MEMS Acoustic Device**
Songsong Zhang, Chengdu Xiansheng Technology/SITRI, China

***14:35-15:05** **Advanced spectral sensing methods for process monitoring applications**
Ray Saupe, Fraunhofer ENAS, Germany

15:05-15:30 **Coffee Break**

15:30-15:50 **TSV INTEGRATED and Pattern Recognition based Multimode Degenerated Low-power 3-dimensional Smart sensing chips**
Simian Zhang, Tsinghua University, China

15:50-16:10 **SPAD-based line sensor IC for chemiluminescence assays in microfluidic channels**
Alexander Zimmer, X-FAB Global Services GmbH, Germany

16:10-16:30 **Newly developed low-reflectivity black resist with high optical density**
Hiroaki Idei, FUJIFILM Corporation, Japan

16:30-16:50 **UV-C Light Detection with High Performance Photodiodes Integrated in a 0.18 µm Modular CMOS Foundry Technology**
Daniel Gäbler, X-FAB Global Services GmbH, Germany

Poster Session:

Design and experiment of a micro planar linear motor equipped with electromagnetic guide
Chao Zhi, Shenzhen Technology University, China

The performance enhancement of CMOS microbolometer with metal-insulator-metal-based plasmonic metamaterial absorbers
Jie Liu, Nanjing University, China

Performance-enhanced CMOS polysilicon microbolometer with narrow supporting arms
Wenbin Zhou, Nanjing University, China

Design of arbitrarily polarized CMOS terahertz detector based on plasmonic antenna
Ke Wang, Nanjing University, China

Investigation of electrical characteristics of a fabricated IGAD detectors at high and low temperatures
Yupeng Lu, Institute of Microelectronics, China

Research on stereo tactile simulation based on microelectrical osmotic pump technology
Li Zheng, Hefei Visionox Technology Co., Ltd, Kunshan Branch, China

An Intelligent General-Purpose Circuit and System for Broad Sensor Array-Based Applications
Junye Li, Shenzhen University, China

Colloidal quantum dot enhanced short-wavelength infrared absorption of avalanche photodetectors
Lilei Hu, Shanghai University, China

A novel multiple guard ring design for low dark current of backscattered electron detectors
Lilei Hu, Shanghai University, China

A Thin Film Cantilever-Based Magnetoelectric Magnetic Field Sensor and Energy Harvester Utilizing the Delta-E Effect
Yuxi Wang, ShanghaiTech University, China

Symposium IX: Design and Automation of Circuits and Systems

Sunday, March 17, 2024Shanghai International Convention Center
Meeting Room: 3E

Session I: Keynote Session I
Session Chair: Weikang Qian, Shanghai Jiao Tong University

13:30-13:35	**Opening Remarks**
	Weikang Qian, Shanghai Jiao Tong University
****13:35-14:05**	**Scale-out Chiplet-based Systems: Architecture, Design and Pathfinding**
	Puneet Gupta, University of California, Los Angeles(UCLA)
****14:05-14:35**	**Photonic-Electronic Design Automation**
	Jiang Xu, Hongkong University of Science and Technology
14:35-14:50	**Coffee Break**

Session II: Design Technology Co-Optimization
Session Chair: Yu-Guang Chen, National Central University

***14:50-15:15**	**Diffusive/Quantum Carrier Transport and Multiphysics Simulation Methods of Advanced Electronic/Optoelectronic Devices**
	Wenchao Chen, Zhejiang University
***15:15-15:40**	**Design Technology Co-Optimization Methods for Advanced Logic Nodes**
	Xingsheng Wang, Huazhong University of Science and Technology
***15:40-16:05**	**Machine Learning for Device Modeling (MLDM) in the DTCO Eco-system**
	Lining Zhang, Peking University
***16:05-16:30**	**Exploring AI-in-the-Loop For Physical Design Verification DFM/DTCO EDA**
	Yongfu Li, Shanghai Jiao Tong University

Monday, March 18, 2024 Shanghai International Convention Center
Meeting Room: 3E

Session III: Keynote Session II
Session Chair: Xunzhao Yin, Zhejiang University

****8:30-9:00**	**Ultra-broadband RF Front-end SoC using 0.18um CMOS technology**
	Jianguo Ma, Zhejiang Lab
****9:00-9:30**	

Session IV: Hardware Security
Session Chair: Xunzhao Yin, Zhejiang University

***9:30-9:55**	**Logic Locking over TFHE for Securing User Data and Algorithms**
	Masanori Hashimoto, Kyoto University
9:55-10:10	**A Customized Model for Defensing Against Adversarial Attacks**
	Jiang Sun, ShanghaiTech University
10:10-10:25	**Coffee Break**

Session V: EDA
Session Chair: Pingqiang Zhou, ShanghaiTech University

***10:25-10:50**	**Logic Synthesis based on Semi-tensor Product of Matrices** Zhufei Chu, Ningbo University
10:50-11:05	**Logic Synthesis for XOR-AND Graphs via Reed-Muller Representations** Zhufei Chu, Ningbo University
11:05-11:20	**Integration of Shift Left Updates into Logic Synthesis and Macro Placement** Xinfei Guo, Shanghai Jiao Tong University
11:20-11:35	**TimingDTH: Timing-driven placement with Deep Three-Head reinforcement learning** Shuai Yuan, Shanghai Jiao Tong University
11:35-11:50	**Decoupling Capacitor Optimization for 2.5D-ICs with Deep Reinforcement Learning Technique** Haiyang Feng, Zhejiang University
11:50-13:30	**Lunch Break**

Session VI: AI Accelertors
Session Chair: An Zou, Shanghai Jiao Tong University

***13:30-13:55**	**Optimizing Architecture and Algorithm for Privacy-Preserving Machine Learning** Jongeun Lee, Ulsan National Institute of Science and Technology
***13:55-14:20**	**Efficient and Robust Hardware for Neural Networks** Li Zhang, Technical University of Darmstadt
***14:20-14:45**	**Algorithm and Hardware Codesign for Brain-inspired Neuromorphic Computing** Aili Wang, Zhejiang University
14:45-15:00	**A Hardware Accelerator for Sparse Computing Based on NVDLA** Yizhou Chen, Zhejiang University
15:00-15:15	**Integer Arithmetic-Based and Activation-Aware GELU Optimization for Vision Transformer** Zihan Zou, Southeast University
15:15-15:30	**Coffee Break**

Session VII: Advanced Circuit and System Design
Session Chair: Aili Wang, Zhejiang University

***15:30-15:55**	**A Journey of High-Density Associative Memories based on Ferroelectric Content Addressable Memories** Xunzhao Yin, Zhejiang University
***15:55-16:20**	**Navigating Aging Effects: Concepts and Implementation in Reliable Computing Systems** Yu-Guang Chen, National Central University
16:20-16:35	**Enhance the Real-Time Performance of FPGA through Partial Dynamic Reconfiguration** An Zou, Shanghai Jiao Tong University
16:35-16:50	**A 16-bit 8MSPS SAR ADC with Configurable Low-Power Comparator** Yidan Liang, Zhejiang University

Poster Session:

Data Flow Graph Partitioning Method for CGRA Temporal Mapping Based on Bayesian Optimization
Yihan Hu, Fudan University

Verification of 400GbE with Optical Modules on an FPGA Platform
C.-Z. CHEN, Peng Cheng Laboratory

A transient enhanced output capacitor-less LDO with adaptive biasing and spike reduction

Qianxi Cheng, Peking University

Design of large-scale power battery safety monitoring system

Zixiang Yan, Hangzhou Dianzi University

DESIGN OF A 10BITS 100MSPS SAR ADC

Chaorun Li, Peking University

Runtime Configurable Approximate Computing System for Simulated Annealing Algorithm

Shi Jian, Shanghai Jiao Tong University

An 18.3~42.1GHz octave frequency tuning class-C quadcore VCO achieving 204.5 dBc/Hz FOMT

Shan Lu, Institute of microelectronics of the Chinese Academy of Sciences

Effective Resistance Estimation for Large Circuits Using Random Walk Algorithm

Jinyu Zhang, Empyrean Technology Co., Ltd.

A Novel Smart Sampling Approach with Broader Compatibility in Semiconductor Manufacturing

Tianyue Lai, Fujian Jinhua Integrated Circuit Co. Ltd.

Designing and Accelerating Spiking Neural Network based on High-level Synthesis

Heng Zi, Beijing University of Posts and Telecommunications

STOCHASTIC COMPUTING HARDWARE DESIGN AND OPTIMIZATION FOR CONVOLUTIONAL NEURAL NETWORKS

Zhinan Chen, Fudan University

A 106TOPS/W SRAM Compute-In-Memory Macro in 28nm with Reconfigurable Bitwise Operation for AI

Yiqi Meng, Zhejiang University

Application of Community Detection based Parallel MOEA/D Algorithm in RF Power Amplifier Circuit Design

Jiejin Zhou, Fudan University

A Hardware Accelerator of the Convolutional Spike Neural Network Based on STDP Online Learning

Qinxin Chen, Zhejiang University

Symposium X: AI & IC Manufacturing

Sunday, March 17, 2024 Shanghai International Convention Center
Meeting Room: 5F

Session I: Modeling & Simulation in Intelligent Systems
Session Chair: Yunlong Li

****13:30-13:55**	**Neuromorphic Audio Edge Intelligence** Shih-Chii Liu, Institute of Neuroinformatics, University of Zurich and ETH Zurich
***13:55-14:20**	**In-memory Computing and Dynamic Vision Sensors: Recipes for tinyML in Internet of Video Things** Arindam Basu, Hongkong City University
14:20-14:35	**A Novel DES Encryption Circuit Based on RRAM XOR Gates** Haoxiong Bi, Zhejiang University
14:35-14:50	**A physical based 2D Monte Carlo Model of MO-ECRAM Programming for Device Optimization** Haotong Zhu, Peking University
14:50-15:05	**Coffee Break**

Session II: Future of Manufacturing: Industrial Insights
Session Chair: Yang Xu

***15:05-15:30**	**AI Empowers Semiconductor Yield Signoff Ecosystem - Reducing Cost and Increasing Efficiency for Manufacturing with a Diversified Supply Chain** Mark Lu, Semitronix Corporation
***15:30-15:55**	**The Application of Virtual Manufacturing in IC Process Development** Yunlong Li, Zhejiang University
***15:55-16:20**	**Depth-first convolution-neural-network pipeline for compute-in-memory architecture** Cimang Lu, Flash Billion
***16:20-16:45**	**Progress of AI for EDA Algorithms** Yu Han, Empyrean Technology Co., Ltd.

Monday, March 18, 2024Shanghai International Convention Center
Meeting Room: 5F

Session III: Exploring Non-von Neumann Architectures
Session Chair: Jinfeng Kang

****8:30-8:55**	**Novel Data Storage Technology for AI** Xiangshui Miao, Huazhong University of Science and Technology
***8:55-9:20**	**Developing a Neuromorphic Computer: Practices and Challenges** Gang Pan, Zhejiang University
***9:20-9:45**	**Heterogeneous integration of analog and digital computing-in-memory technologies** Shaodi Wang, WITMEM Co., Ltd.
9:45-10:10	**The Integration of AI Large Model & Neuromorphic Computing in Memory with High Speed Analog Ics** Hongjie Liu, Shenzhen Reexen Technology Co., Ltd.
10:10-10:25	**Coffee Break**

Session IV: Co-optimization from Technology, Device to Design
Session Chair: Cheng Zhuo

***10:25-10:50**	**Nonvolatile emerging memory devices for energy-efficient edge AI accelerators** Daniele Ielmini, Politecnico Di Milano
***10:50-11:15**	**Snapdragon Platform for High Performance 5G Mobile SOC & AI/Computing Application Manufactured with 4nm EUV Fin-FET Technology and Beyond** Jun Yuan, Qualcomm
***11:15-11:40**	**Large Scale VLSI Mask Optimization** Bei Yu, The Chinese University of Hong Kong
11:40-11:55	**Universal Process Migration Solution of MAGICAL for Analog IC Layout Automation** Yufeng Wei, Fudan University
11:55-13:30	**Lunch Break**

Session V: AI Innovations in Semiconductor Manufacturing
Session Chair: Ye Lu

***13:30-13:55**	**Deep Neural Network Proxy Modelling for IC Virtual Fabrication** Dong Ni, Zhejiang University
13:55-14:10	**A SelectiveNet-based Method for Defect Classification in Semiconductor Manufacturing** Qian Jin, Zhejiang University
14:10-14:25	**AI driven process control by machine learning based virtual metrology for high product mix manufacturing** Chunshan Du, Siemens EDA
14:25-14:40	**Machine Learning Technologies for Semiconductor Manufacturing** LiFei Sun, Lam Research
14:40-14:55	**Deep-Learning-Based Proxy Modeling for Microscopic Process of Plasma Etching** Shuhang Chen, Zhejiang University
14:55-15:10	**Predicting Material Removal Rate in Chemical Mechanical Polishing (CMP) Using Explainable Machine Learning Methods** Jiahui Zuo, Zhejiang University
15:10-15:25	**Coffee Break**

Session VI: Advancements in Semiconductor Materials and Devices
Session Chair: Dong Ni

***15:25-15:50**	**Research on the application of artificial intelligence in device compact model and technology – circuits co-optimization** Ye Lu, Fudan University
***15:50-16:15**	**Vector Matrix Multiplication with Two-Dimensional Materials** Mario Lanza, KAUST
16:15-16:30	**α-In_2Se_3/$MoTe_2$ heterojunction for p-type junction field-effect transistors with ferroelectric memory characteristics** Tianjiao Zhang, Zhejiang University
16:30-16:45	**Investigation of the Carrier Velocity in Short Channel Ge MOSFET with NiGe Metal Source/Drain** Jing Yan, Zhejiang University
16:45-17:00	**A First-Principles Study on the Stable Phase in Yttrium-Doped HfO_2** Xiaomin Xiao, Peking University
17:00-17:15	**Tiny Neural Network Representing MOSFET Physical Effect Sub-model** Shuhan Wang, Peking University

Poster Session: **High-speed performance testing strategy and solution for AI wave**

Zhexi Yan, ADVANTEST

Metal-Oxide-Metal Capacitor Simulation and Modeling by Virtual Fabrication

Qingpeng Wang, Lam Research

APPLICATION OF ADVANCED PROCESS CONTROL FOR IC MANUFACTURING

Linglie Zeng, Ontoinnovation

Study of Defectivity and Yield Impact from the Establishment and Optimization of FOUP Clean and FOUP Use Routine in Advanced IC Manufacturing

Zhigang Zhang, Brooks Technology (Shanghai) Limited

Anomaly Detection of CDSEM Images

Meng Xue, Shanghai Huali Microelectronics Corporation

PMOS leakage reduction through SiGe morphology & IMP profile fine tune

WenZhao Fu, Shanghai Huali Integrated Circuit Corporation

The Defect Formation and Reduction of 55NM Ultra-low Power (55ULP) BEOL Process

Qing Mao, Shanghai Huali microelectronics Corporation

A Novel GAN-based Data Augmentation Algorithm for Semiconductor Defect Inspection

Lilei Hu, Shanghai University

Simulation and study of the interaction between needle mark morphology and probe card

Chenxi Zhao, Shanghai Huali integrated Circuit Manufacturing Co., Ltd.

CONVOLUTIONAL NEURAL NETWORK (CNN) BASED PROCESS WINDOW ANALYSISING FOR LITHOGRAPHY

Zeyang Chen, School of Micro-Nano Electronics, Zhejiang University

Structure Optimization of NOR Flash for Improving Cell Performance

Jiayu Ma, Shanghai Huali Integrated Circuit Corporation

Improved EM Performance by Adjusting Etching Profile of Top Metal for 28HK Metal Gate Process

Zherui Cao, Shanghai Huali Integrated Circuit Co., Ltd.

Digitalization Solutions for Automated Material Handling Systems in Semiconductor Smart Factories

Ruiji Wang, Huaxin (Jiaxing) Intelligent Equipment Co., Ltd.

High-Performance of SOT-MRAM Based on Optimization of Integration Processes

Xiaofei FAN, Truth Memory Corporation

A novel deep neural network based algorithm for fast wafer effective carrier lifetime measurement using heterodyne lock-in carrierography

Lilei Hu, Shanghai University

A method for predicting the film thickness of IC deposited films based on FCBF-CatBoost

Cai Yu, University of Science and Technology of China

55NM ULTRA LOW LEAKAGE PLATFORM DEVELOPMENT

Yifan Ding, Shanghai Huali Microelectronics Corporation

High Performance Wafer Defect Classification Model Based on Feature Fusion and RGB SEM images

Zhongyu Shi, University of Science and Technology of China

DSA for Nickel Silicide Formation in Advanced Devices

Haifeng Zhu, Applied Materials

Surface Damage Matching between VIISta 550H and VIISta 1500H

Huang Zeng, Applied Materials

Model of Organic Ferroelectric Transistors for Neural Networks

Kairui Ding, Nanjing University of Posts and Telecommunications