HUA TIAN 华天科技（昆山）电子有限公司
HUATIAN TECHNOLOGY(KUNSHAN)

New Technology Release Huatian-Sumacro “Embedded Silicon Fan-out (eSiFO®) Technology and Product”

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Huatian Group

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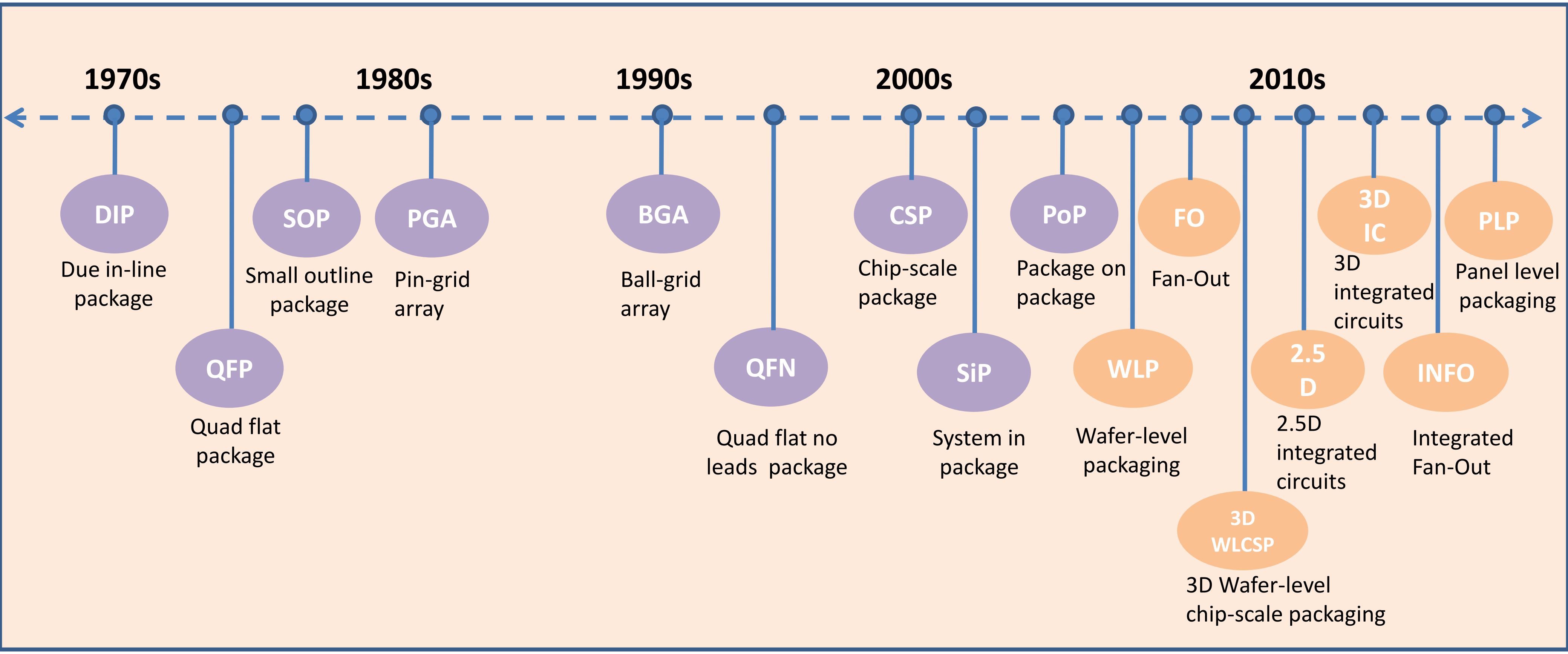
Sumacro

2018 March 16

1 Application Driving Packaging Development

Mobile	IoT	Auto	Computing	Big data
•Ultra thin, small •Integration, SiP •5G	•Miniaturization •Integration •Secure •Power •Home/fact./Auto	•Reliable, AEC-006 •Integration, SiP •MEMS/Sensor •5G •ADAS •Infotainment/ECU	•Performance •Integration •Thermal •Power •Data center/SiPHO	•Performance •Thin die stacking •Reliability •Cloud •3D NAND

2 Evolution of Packaging Technology



1970s

DIP Due in-line package

QFP Quad flat package

SOP Small outline package

1980s

PGA Pin-grid array

1990s

BGA Ball-grid array

QFN Quad flat no leads package

2000s

CSP Chip-scale package

SiP System in package

PoP Package on package

WLP Wafer-level packaging

FO Fan-Out

2010s

3D WLCSP 3D Wafer-level chip-scale packaging

2.5 D 2.5D integrated circuits

3D IC 3D integrated circuits

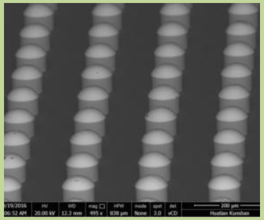
INFO Integrated Fan-Out

PLP Panel level packaging

- ✓ A number of new technologies were developed since 2000s
- ✓ Advanced packaging technologies: WLP, FO, 3D WLCSP, 2.5D, 3DIC, 3D FO etc.
- ✓ TSV and FO are very meaningful for ultra small and low profile package.

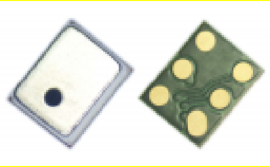
3

Advanced Packaging Platform of Huatian Group



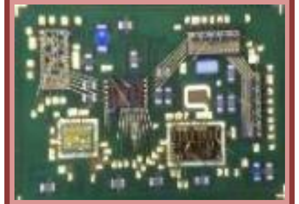
Flip Chip Bumping

Lamiante/
wafer



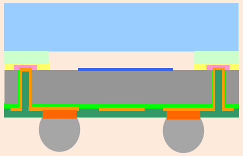
MEMS

Laminate/
Leadframe/
Wafer



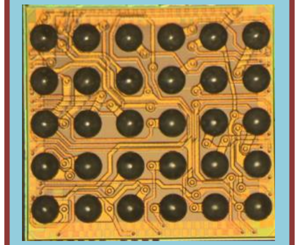
SiP

Laminate



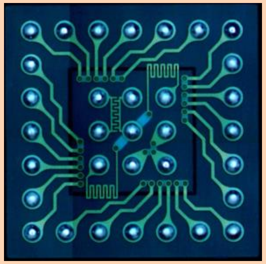
TSV

Wafer



Chip Scale Packaging

Wafer



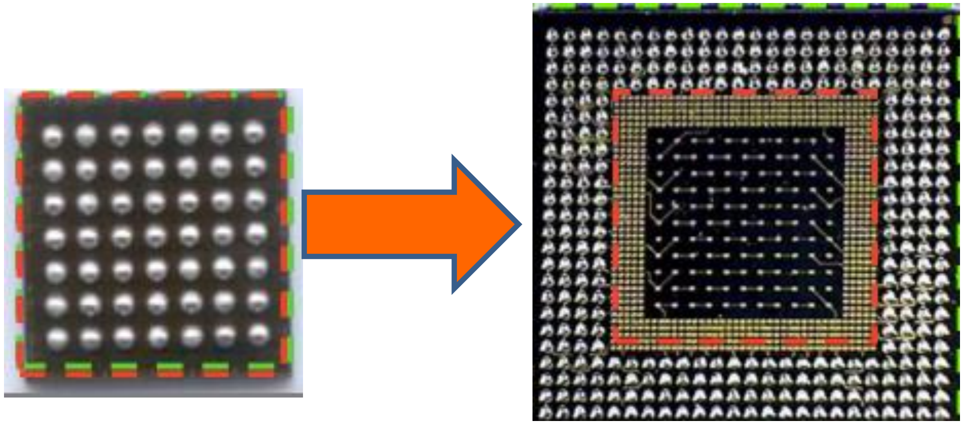
Next Gen SiP（FO)

Wafer

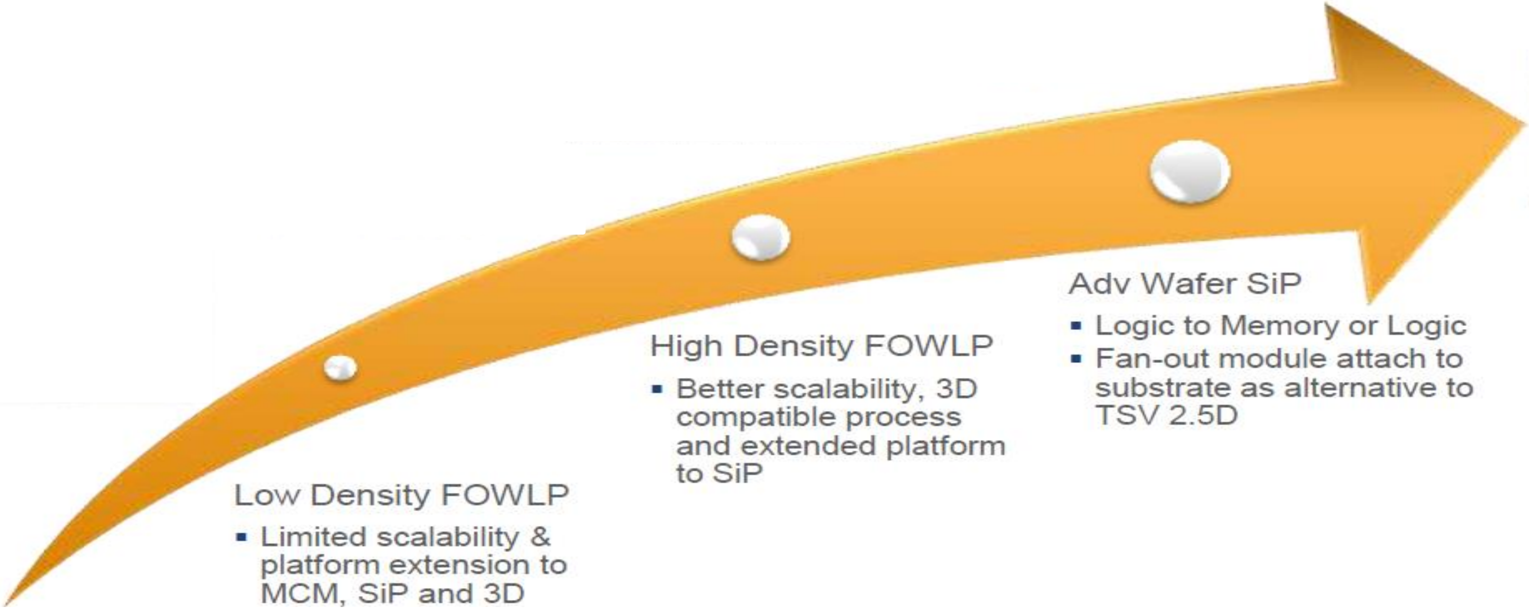
- ✓ Huatian has develped advanced packaging technologies: FC/Bumping, MEMS, SiP, 3D WLCSP, 3D FO etc.

4

From Fan-in to Fan-out



- ☐ Fan-in :
  - ☐ Chip scale packaging
  - ☐ Chip size determine BGA pitch
  - ☐ Single die package
- ☐ Fan-out :
  - ☐ Package size no limit
  - ☐ Ball pitch no limit
  - ☐ Suitable for multi-die integration



Miniaturization
Integration
Performance
Reliability
Cost

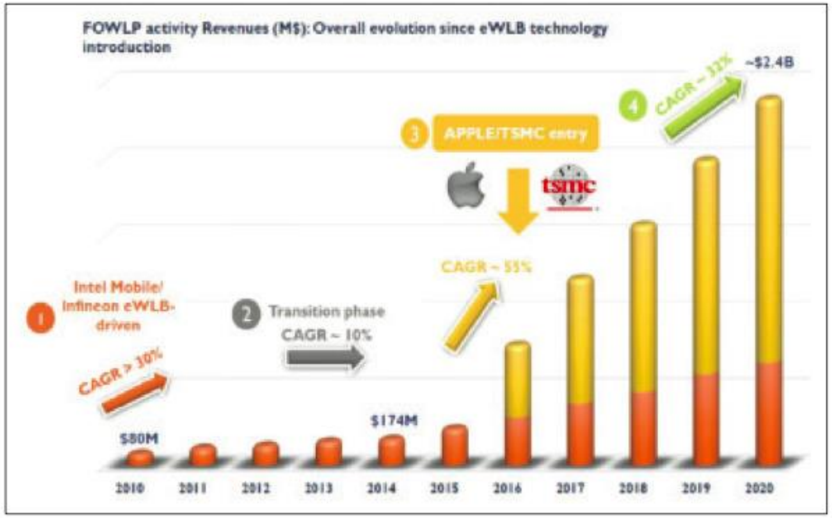
Low Density FOWLP
- Limited scalability & platform extension to MCM, SiP and 3D

High Density FOWLP
- Better scalability, 3D compatible process and extended platform to SiP

Adv Wafer SiP
- Logic to Memory or Logic
- Fan-out module attach to substrate as alternative to TSV 2.5D

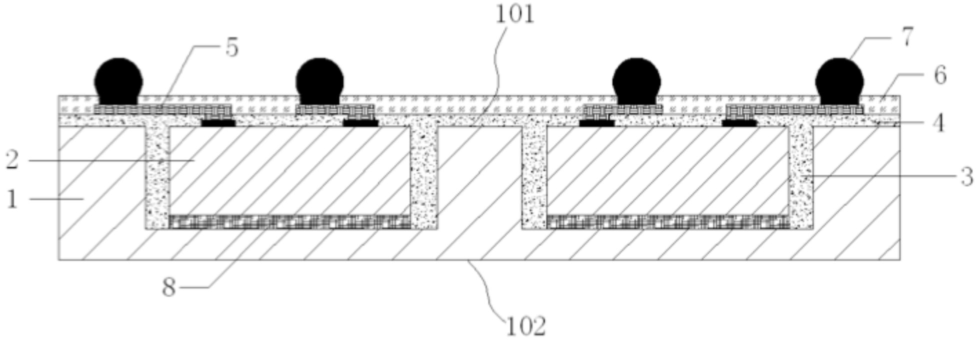
5 Application of WLP-FO

- Baseband Processors 基带处理器
- RF Transceivers 射频收发器
- Power management integrated circuits (PMIC)电源管理芯片
- Connectivity 通讯模块
- 77GHz ADAS Radar module for automotive
  应用于汽车驾驶辅助、安全系统的77GHz毫米波雷达模组
- mmWave MMIC毫米波芯片（5G芯片）
- Near field communication (NFC) 近场通讯
- Audio CODEC 音频解码器
- Security devices 安全器件
- Microcontrollers (MCU) 单片机
- Memory 存储
- NAND memory controllers 闪存控制器
- Touchscreen controller 触摸屏控制器
- RF-MEMS Tuner 射频微机电系统调谐器
- Sensors 传感器
- Bio/Medical devices 生物/医疗器件
- Application processors 应用处理器

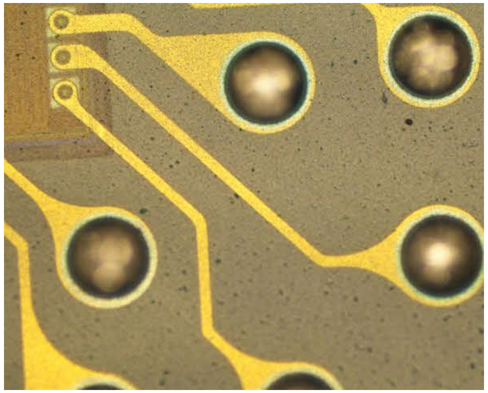


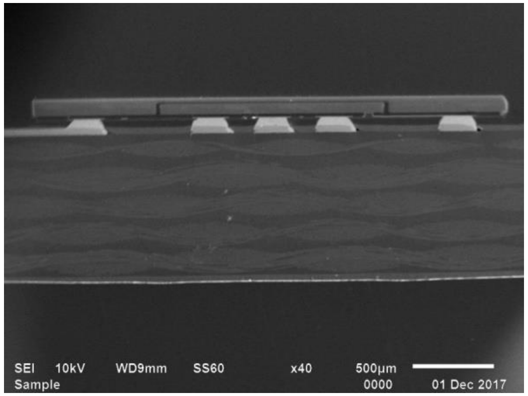
"Status of the advanced packaging industry" www.i-micronews.com

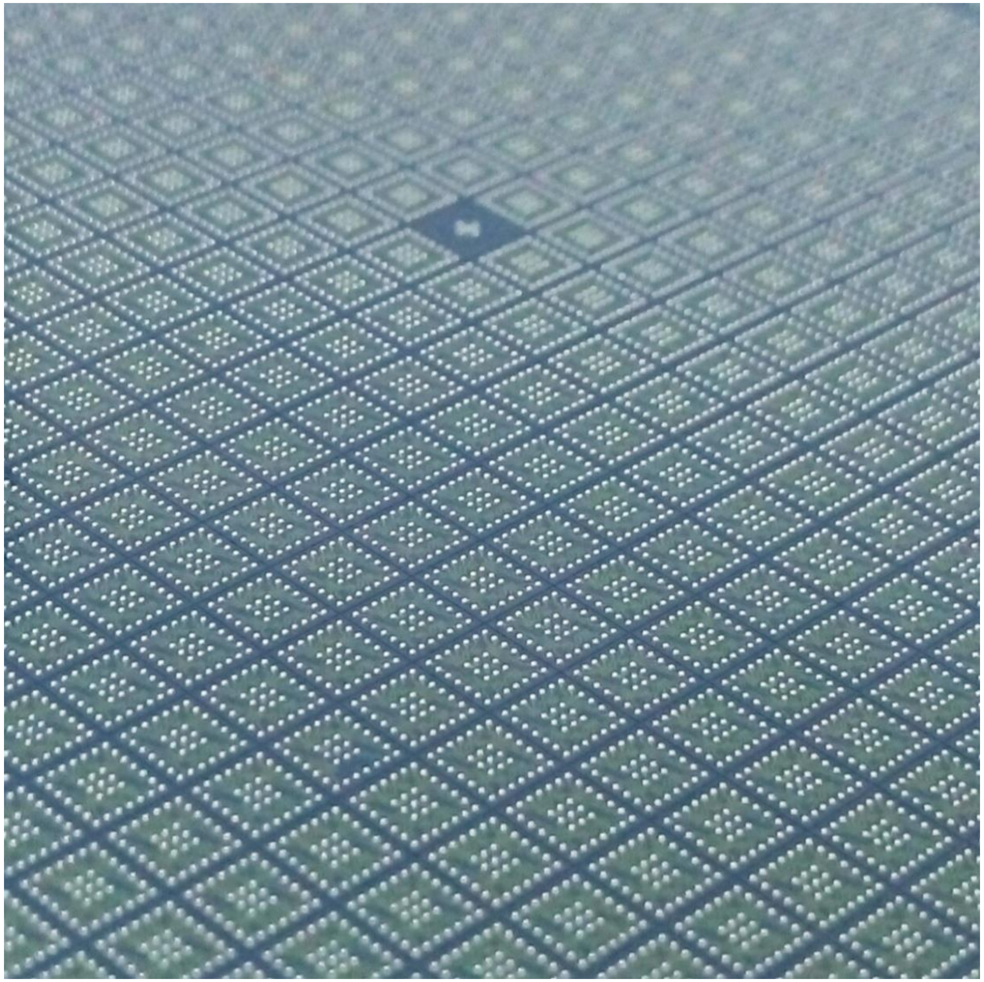
Huatian embedded Si Fan-Out(eSiFO®)



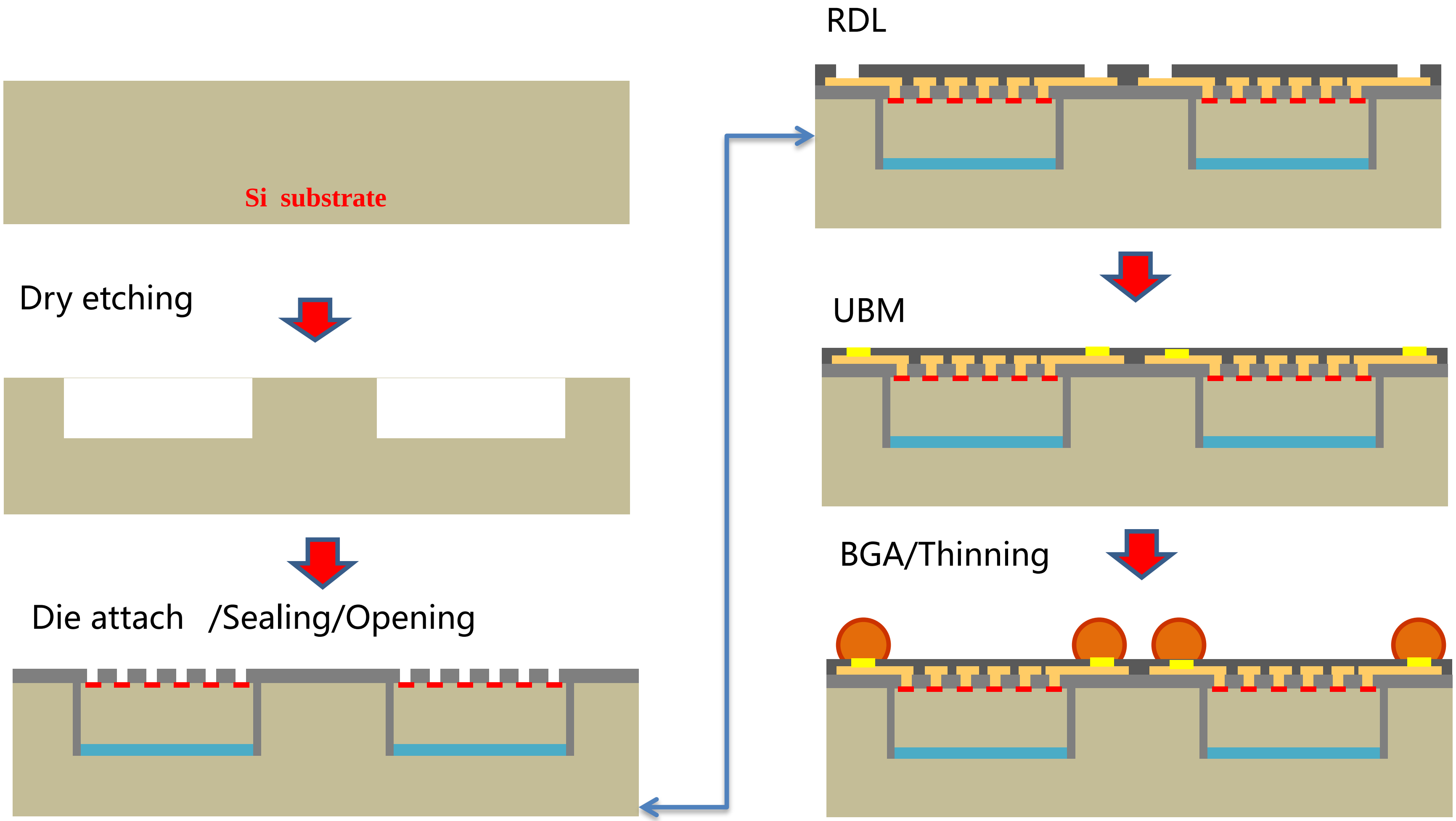
- ✓ KGDs embedded in silicon wafer;
- ✓ Micro-scale gap is filled by epoxy;
- ✓ Silicon surface as the FO area.







Process of eSiFO®



Dry etching

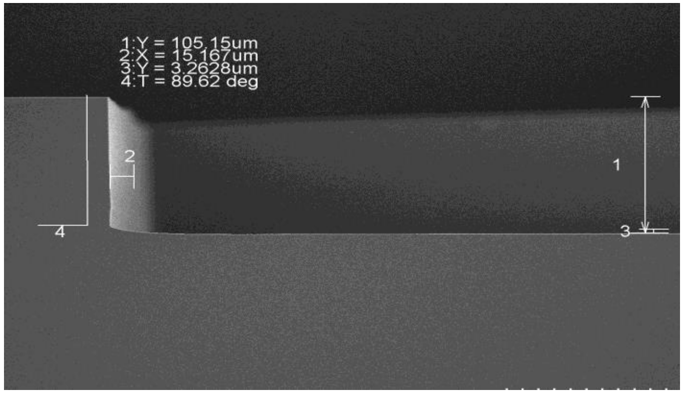
Die attach /Sealing/Opening

RDL

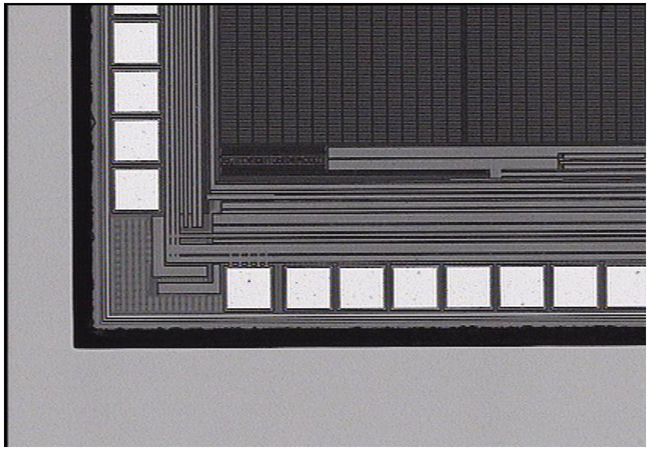
UBM

BGA/Thinning

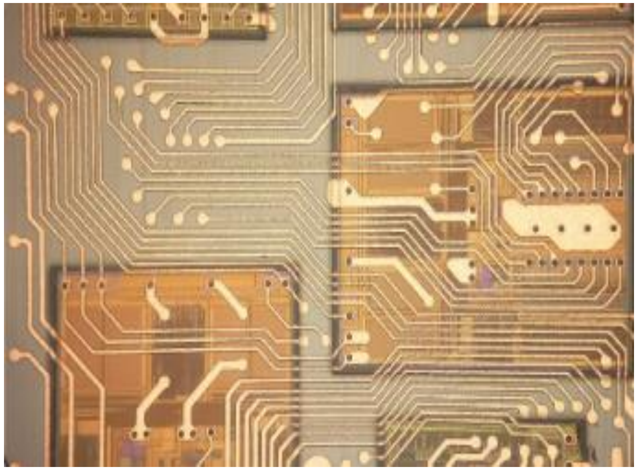
Process Results



- TTV≤4um for 100um etch depth



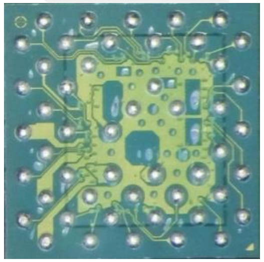
- Pick place accuracy ≤4um



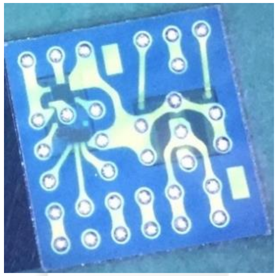
- ~RDL with 15um L/S

9 Development Milestones

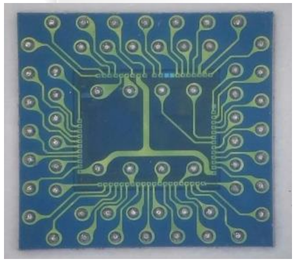
2015.08
First patent file



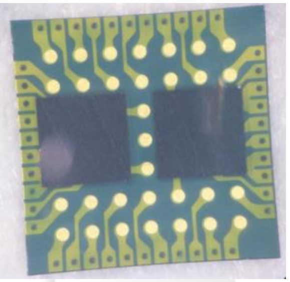
2016.03
Dummy prototype



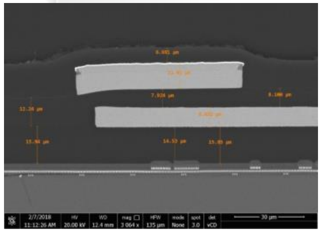
2016.08
First SiP delivered



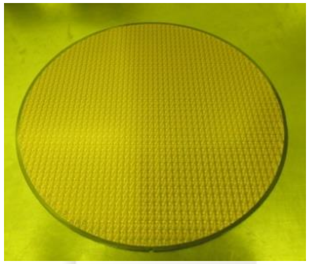
2017.05
First products delivered



2017.08
3D eSiFO process developed



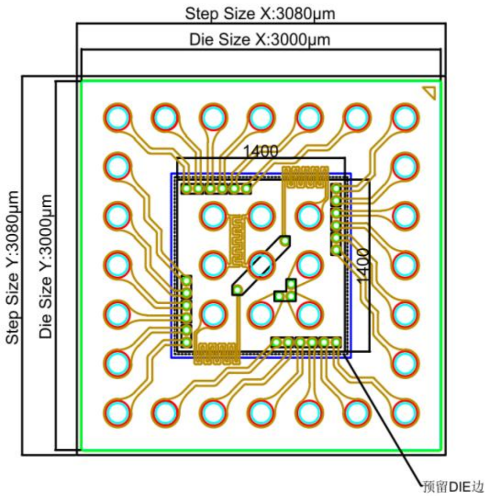
2017.09
2 RDLs products developed

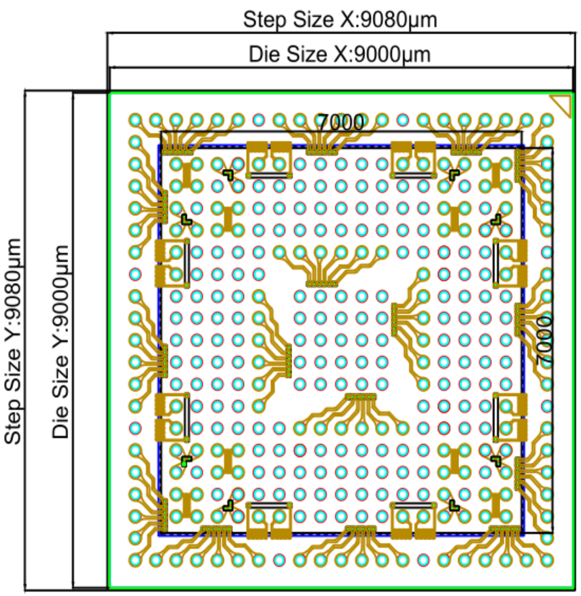


2018.03
12 inch process developed

10 Package Level Reliability

- **Test vehicles**

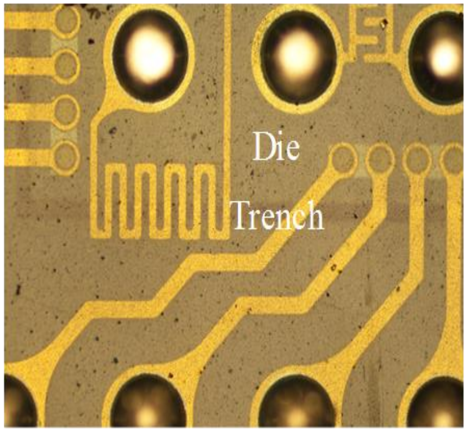


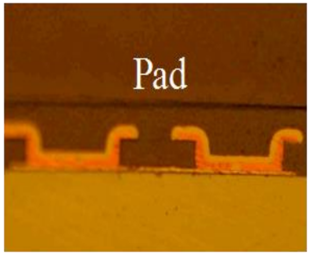


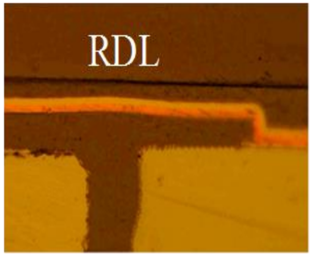
Specification	Test vehicle	
Package type	eSiFO	
Package size	3 × 3 mm	9 × 9 mm
Die size	1.4 × 1.4 mm	7 × 7 mm
Body package height	150um	200um
BGA diameter / pitch	0.2 mm / 0.4 mm	
RDL layer / dielectric layer	One RDL layer / Two dielectric layers	
Daisy chain unit	12	48
Kelvin test unit	1	8
Leakage current test unit	1	8
RDL reliability test unit	2	16

- **Results**

Reliability test	**JEDEC specification**	**Test condition**	**Results**
Pre-conditioning	JEDECJ-STD-020D	125℃, 30 ℃/ 60%RH, 3 x Reflow	Passed
THS	JESD22-A101	85℃/85%RH	Passed
TC	JESD22-A104	-55/125℃	Passed
HAST	JESD22-A118	110℃/85%RH	Passed

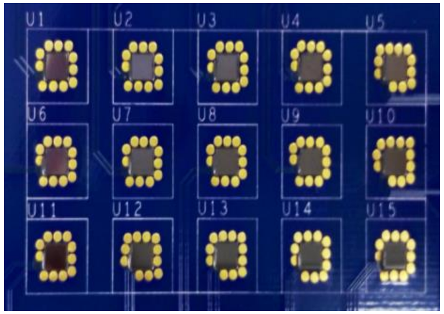


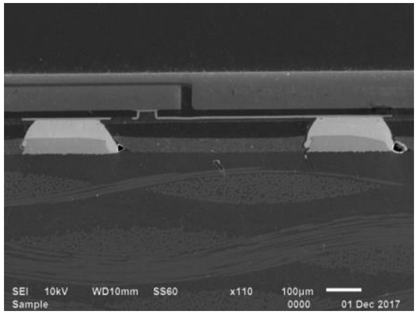




- ➢ All the samples have successfully passed the reliability test.
- ➢ No cracks or delamination after the reliability test !

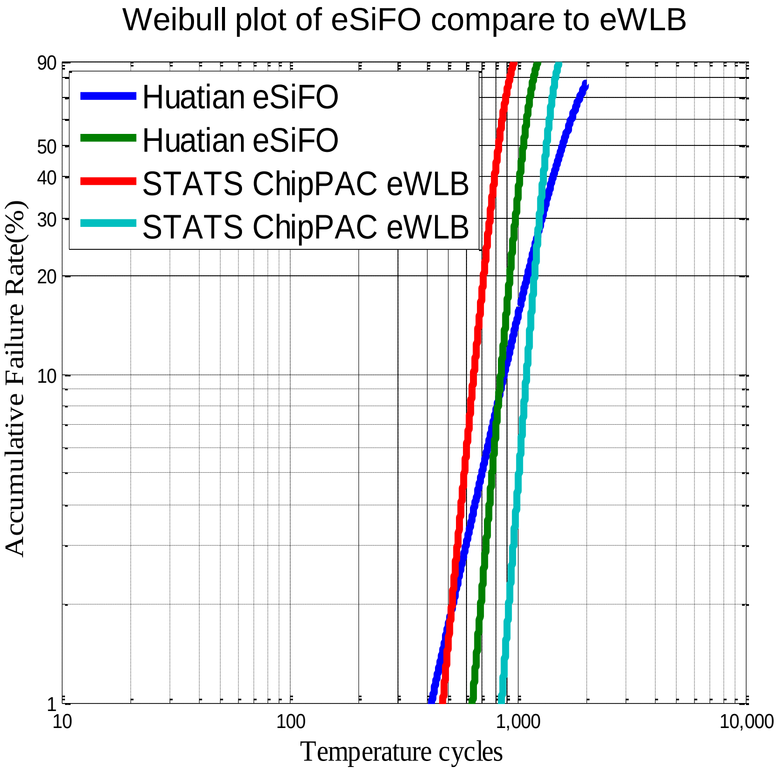
11 Board Level Reliability



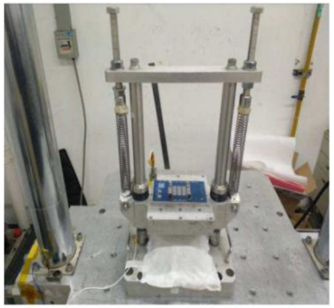


- **Temperature cycling**

No.	Test vehicles		Test condition	Life (63.2% fail)
1	3 × 3 mm	Without underfill	-40℃/125℃	1773
2	3 × 3 mm	With underfill	-40℃/125℃	5893
3	9 × 9 mm	Without underfill	-40℃/125℃	662
4	9 × 9 mm	With underfill	-40℃/125℃	2464



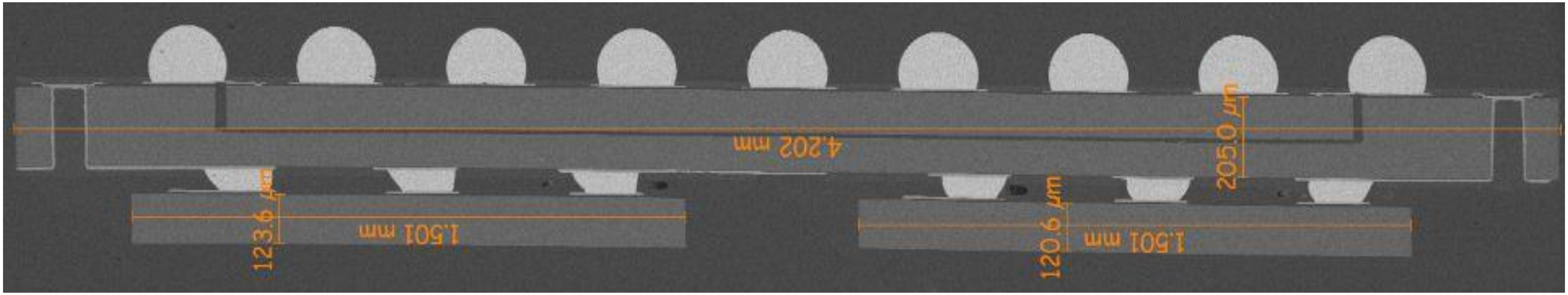
- **Drop test**



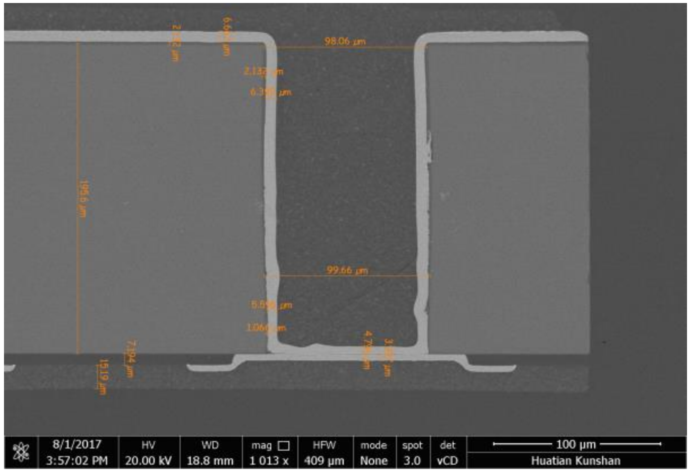
No.	Test vehicles		Test condition		Results
1	3 × 3 mm	Without underfill	1500g, 0.5ms	30 drops	Passed
2	9 × 9 mm	Without underfill	1500g, 0.5ms	30 drops	Passed

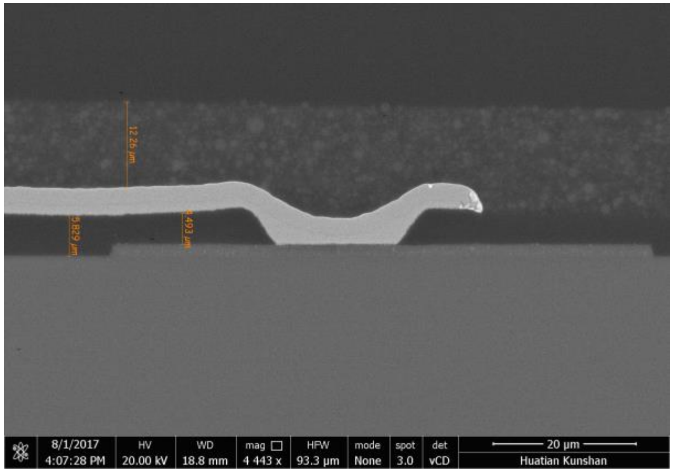
- ➢ eSiFO have similar solder joint fatigue life compared to eWLBs.
- ➢ eSiFO successfully passed 30 board level drops， acceptable for mobile applications.

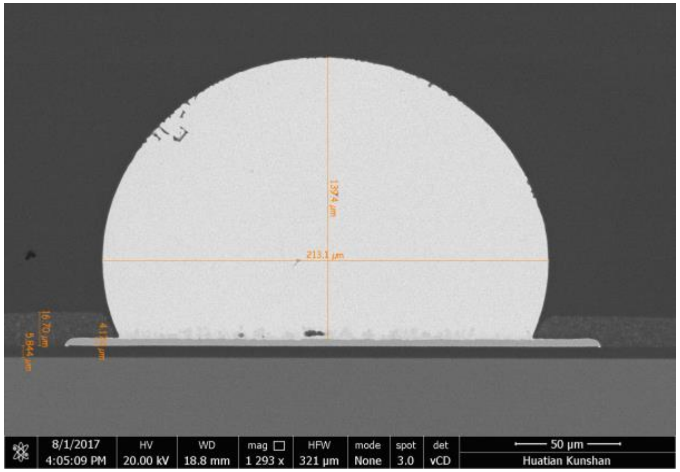
3D eSiFO-SiP



- ☐ 3D embedded Silicon integration using via last TSV for vertical interconnects







- ☐ 3D eSiFO-SiP can be used for processor+ memory, sensor+ASIC, MEMS+ASIC

Advantages of eSiFO®

- Easy to realize multi-chip SiP
- Ultra small and low profile package (~150µm)
- Ultra Fine pad pitch for embedded chip (<60µm)
- Small distance between embedded chips (<30µm)
- Compatibility with standard WLP process
- Better thermal and good electrical performance
- Function wafer with blank area for die embedding
- Fabrication of device on embedded wafer
- Heterogeneous integration
- Simple process: no molding, de-bonding
- Low warpage
- Low cost, especially for multi chip SiP
- Flexible package type: WLP/BGA/LGA/QFP
- 3D integration with TSV
- Reliability

Roadmap of eSiFO®

itmes	2017	2018	2019	2020
Die size (mm)	0.6x0.6~7x7	0.5x0.5~7x7	0.4x0.4~9x9	0.3x0.3~12x12
Pad pitch (in µm)	≥60um	≥55um	≥50um	≥45um
Pad size(in µm)	≥45um	≥40um	≥40um	≥40um
Min. RDL (L/S) (in µm)	10	7	5	2
RDL Layers	2	3	4	4
Package size	1x1~8x8	0.8x0.8~12x12	0.8x0.8~15x15	0.8x0.8~15x15
Package body thickness (in µm)	200	150	120	100
3D Fan-Out	sample	Available	Available	Available
Electroless Plated UBM	Ni/Au or Cu	Ni/Au or Cu	Ni/Au or Cu	Ni/Au or Cu
Min. BGA height	100	90	80	80

Honor

集成电路产业技术创新战略联盟创新奖

奖项类别：技术创新奖

获奖单位：华天科技（昆山）有限公司

获奖项目：华天晶圆级硅基扇出型封装技术研发团队

获奖项目：硅基扇出型封装技术

二零一八年三月

The eSiFO® technology received ICIA’ S first Technology Innovation Award, and was regarded a significant achievement on leading edge advanced packaging field.

Huatian-Sumacro Joint Development

- Second largest in revenue/market value of the largest Chinese backend Assembly & Test manufacturer). Six Manufacturing Sites with approx. 13,000 staff globally..

- A leading IC design company on LED controller and driver located in Suzhou.

Honor of Driver IC From Sumacro

荣誉证书

苏州日月成科技有限 公司

贵司"SUM2017系列LED显示驱动IC"荣获"2015中国LED首创奖"

金奖

特颁此证，以资鼓励

中国照明学会
半导体照明技术与应用专业委员会
二0一五年四月二十三号

荣誉证书
HONORARY CREDENTIAL

苏州日月成科技有限公司

贵司 SUM2035系列LED显示驱动IC

荣获"第四届中国LED首创奖"：

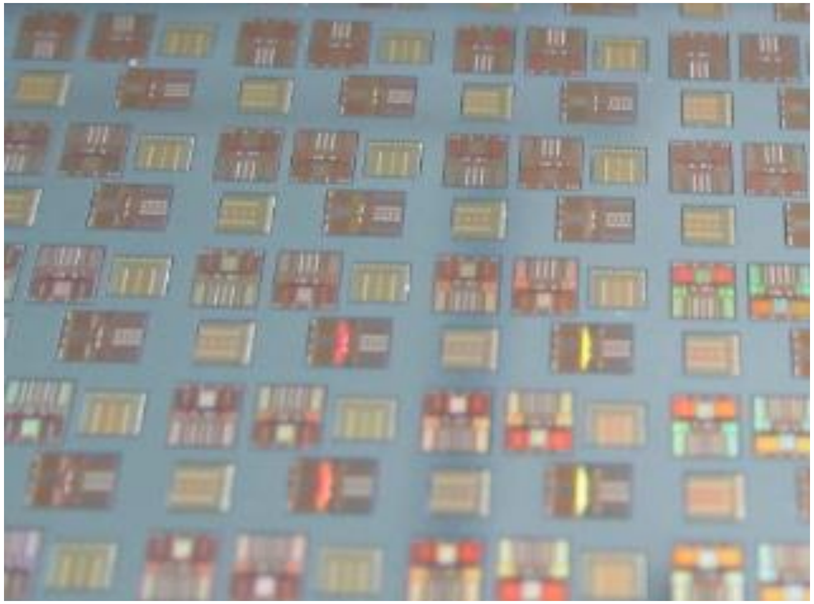
金 奖

特颁此证，以资鼓励

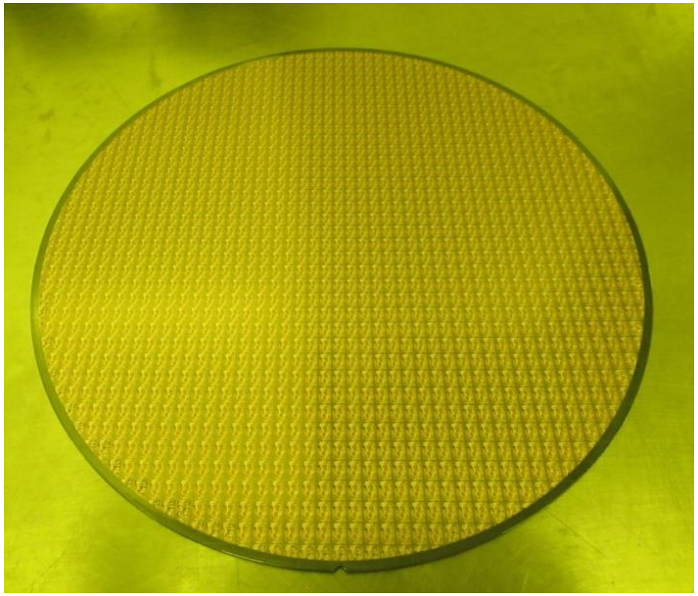
中国照明学会
半导体照明技术与应用专业委员会
二零一七年四月二十二号

○ More than 20 years experience for LED display marketing and innovation. Experts in high grayscale depth, high fresh rate, advanced power save technology, true color display etc.

Joint Development eSiFO® Products



Multi-die embedded Silicon Integration



- **12 inch BGA**

- Multi-chips were integrated in an ultra small silicon die.
- 12 inch process was developed.
- The advantages using eSiFO® for LED controller and drivers are high display performance, advanced Power Save technology applied to HD LED display of high resolution, simple SMT, good cost performance value..

Acknowledgement

- We would like to express their gratitude to the great support and collaboration from our vendors and customers!
- Especially, we appreciate equipment supplier ASM Pacific for their two years' great support!
- We would like to thank the support from various teams at different locations within Huatian Group!

ASM Pacific Technology

2018 THOMSON REUTERS
TOP100
GLOBAL TECH LEADER

FIREBIRD (TCB)

ORCAS (Wafer & Panel Level Encapsulation)

NUCLEUS (Precision WLP & PLP)

Most comprehensive and unparalleled AP product portfolio
Strategically engaging in key processes w/ good growth

ICA 1205 (Laser sawing & grooving)

FT-MICRO (Test Handler)

SUNBIRD (Test & Pack)

HUA TIAN

THANK YOU

Looking forward to Win-Win Cooperation