Packaging Technologies for Flash Memory

Steve X. Liang, SVP/CTO

3/2017@Semicon China, Shanghai
• Worldwide Semiconductor and Memory
• China’s Memory Industry Growth
• 2D to 3D NAND Ramping-Up
• Packaging Technologies for Memory
• JCET Memory Packaging Portfolio
Global Semiconductor and Memory Market

Memory Contributes To One-fourth Of World Wide Semiconductor Consumption

Source: Micron / Gartner 4Q15
Explosive Data Growth

1 ZB = $10^{21}$ bytes = 1000,000,000,000,000 GB

“BIG DATA” Creation Is Taking Place Due To Wide Spread Deployment In Mobile/Computing Applications. Data Is The New “Oil” In The Next Decade.

Source: Three Reasons why Solid State Drives will take over Hard Drives in 2016 – HP & Samsung
NAND Flash Applications and Growth Drivers

- >500M Tweets / day
- >8.7B Pages / day
- >50B Messages / day
- >1.2B Messages / day
  Phones Checked

Increase in Cloud storage - “BIG DATA”

By 2020 >50B things will be connected...
...And they will all need flash

CARS – Navigation, Infotainment, etc
SSD replacement of HDD due to lower cost of 3D NAND

Larger Camera resolution (12 Megapixel)

100M+ “Selfies” Taken / Day

Wearable Memory

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China’s Memory Consumptions

Chinese Domestic DRAM And NAND Flash Consumption Is Dramatically Increasing With The Rise Of PCs Smartphones. China Consume ~ 30% Of World’s Memory Production And Most Of Them Are Imported

Source: TrendForce, Oct 2015
China’s NAND Flash Significant Growth

China’s NAND Flash wafer capacity, 2015 Vs 2020

2015: XMC+Unisplendour - 80, Samsung Xian+Intel Dalian - 5
2020: XMC+Unisplendour - 420, Samsung Xian+Intel Dalian - 170

Source: Trendforce, Apr 2016
Memory Device Technology Advance

SAMSUNG NAND Wafer node scaling
- 120nm 128 MB
- 90nm 256 MB
- 70nm 512 MB
- 60nm 1 GB
- 50nm 2 GB
- 40nm 4 GB

INTEL NAND Wafer node scaling
- 130nm 128 MB
- 90nm 512 MB
- 50nm 1 GB
- 34nm 4 GB
- 25nm 8 GB
- 16nm 16 GB

3D (48L) 32 GB


3D NAND Technology Provides Economic Benefits Of Scaling Significantly Drive Down $/Bit Cost
3D NAND – A Packaging Concept?

BiCS 3D-NAND

5) Replicate

6) Make contact to staircase vias

Note: Diagram not to scale
## 3D NAND Ramping Up

<table>
<thead>
<tr>
<th>Manufacturers</th>
<th>2012</th>
<th>2013</th>
<th>1H14</th>
<th>2H14</th>
<th>1H15</th>
<th>2H15</th>
<th>2016</th>
<th>2017</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Samsung</strong></td>
<td>21 nm</td>
<td>24 L</td>
<td>6 nm</td>
<td>TLC</td>
<td>14 nm</td>
<td>12(10) nm</td>
<td></td>
<td></td>
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<tr>
<td><strong>Toshiba</strong></td>
<td>24 nm</td>
<td>19 nm</td>
<td>A-19 nm</td>
<td>TLC</td>
<td>15 nm</td>
<td>12(10) nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Micron</strong></td>
<td>20 nm</td>
<td>16 nm</td>
<td>TLC</td>
<td>SSD</td>
<td>12 nm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SK hynix</strong></td>
<td>25 nm</td>
<td>20 nm</td>
<td>16 nm</td>
<td>TLC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SanDisk</strong></td>
<td></td>
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</tr>
</tbody>
</table>

**Note:** The table above shows the evolution of 3D NAND technologies across different manufacturers from 2012 to 2017, with a focus on node sizes and capacity levels for SSD and TLC storage types.
# Memory and NAND Packaging

## REMOVABLE
- SD - SiP
- USB-SiP
- MicroSD

## MOBILE / WEARABLE
- Single chip eWLB
- UFS
- eMMC
- eMCP

## CLIENT SSD
- FLIP CHIP (SSD Controller)
- FBGA-SD

## ENTERPRISE SSD
- FBGA-SD

## AUTOMOTIVE
- SD - SiP
- TSOP
- MicroSD

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Overview of JCET Group

- Founded in 1972 and listed on Shanghai Stock Exchange in 2003
- Largest OSAT in China and 3rd largest OSAT in the world
- Significant manufacturing scale with factories strategically located in China, Singapore and Korea
- Comprehensive product portfolio from discrete, wirebond and flip chip packages to advanced wafer level and System-in-Package (SiP) solutions
- Experienced R&D team driving innovations in advanced technologies with the largest Intellectual Property (IP) portfolio in the OSAT industry
Global Footprint in Strategic Semiconductor Hubs

Morges, Switzerland

Suqian, China

Incheon, S. Korea

Chuzhou, China

JCET Group Corporate Headquarters
Jiangyin, China

Singapore

Fremont, CA
San Diego, CA
Tempe, AZ

Manufacturer / Test Facilities
R&D Centers
Sales Presence

Zoom in on China factory locations
Significant Manufacturing Scale

1. Campus 1: JCET HQ, JCAP B1
   - Middle Binjiang Road, Jiangyin
   - 61K m² / 661K ft² mfg
   - Bumping, wafer level pkg & test

2. Campus 3: SiP, MISpak, JCAP B2, Xinshun, SJsemi and JSCC
   - Changshan Road, Jiangyin
   - 187K m² / 2,010K ft² mfg
   - SiP, MISpak, flip chip, leaded, laminate, bumping, WL CSP, test & MIS

3. China (SCC)
   - Quingpu District, Shanghai
   - 91K m² / 983K ft²
   - Leaded, laminate, stacked die, flip chip & memory cards
   - Relocating to Jiangyin by Sep 2017 (JSCC)

4. Power Package Factory
   - Suzian, Jiangsu Province
   - 50K m² / 538K ft² mfg
   - Power package and test

5. Low Power Discrete Factory
   - Chuzhou, Anhui Province
   - 120K m² / 1,292K ft² mfg
   - Leaded, discrete package and test

6. South Korea (SCK2, SCK3, SCK4)
   - Incheon (IFEZ)
   - SCK3/3+: 227K m² / 2,445K ft²
   - SCK2: 20K m² / 212K ft²
   - SCK4: 7.5K m² / 81K ft²
   - Flip chip, Laminate (CSP, stacked die), SiP, pre-stack, SLT & final test

7. Singapore (SCS)
   - Yishun
   - 75K m² / 808K ft²
   - Advanced wafer level package, laminate, QFN & test

8. Singapore (SCS-WD)
   - Woodlands
   - 4.75K m² / 51K ft²
   - R&D Center
Strongest IP Portfolio in OSAT Industry

Patents Issued by the US Patent & Trademark Office
As of December 2016

- JCET Group: 1673
- Amkor (with J-Device): 915
- ASE: 867
- SPIL: 517

Patents Issued by the State Intellectual Property Office of China
As of December 2016

- JCET Group: 1190
- Amkor (with J-Device): 4
- ASE: 651
- SPIL: 147

Source: Based on Patent Information Published in USPTO Website and State Intellectual Property Office of China

- Leading the OSAT industry with highest number of issued patents
- Over 68% of US patents are related to advanced wafer level and flip chip technology
Patent Innovations Ranked among the Top 20 Semiconductor Equipment Manufacturing Companies Worldwide

<table>
<thead>
<tr>
<th>Company/Organization</th>
<th>Country of Headquarters</th>
<th>Pipeline Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Applied Materials Inc.</td>
<td>United States</td>
<td>1,165</td>
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<tr>
<td>Lam Research Corp.</td>
<td>United States</td>
<td>771</td>
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<tr>
<td>V Technology Co.</td>
<td>Japan</td>
<td>669</td>
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<tr>
<td>Novellus Systems Inc. (Lam Research Corp.)</td>
<td>United States</td>
<td>487</td>
</tr>
<tr>
<td>ASM International NV</td>
<td>Netherlands</td>
<td>319</td>
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<tr>
<td>KLA-Tencor Corp.</td>
<td>United States</td>
<td>253</td>
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<tr>
<td>Tokyo Electron Ltd.</td>
<td>Japan</td>
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<tr>
<td><strong>Stats ChipPac Ltd.</strong></td>
<td>Singapore</td>
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<td>ASML Holding NV</td>
<td>Netherlands</td>
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<td>ATMI Inc.</td>
<td>United States</td>
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<tr>
<td>Advanced Semiconductor Engineering Inc.</td>
<td>Taiwan</td>
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<tr>
<td>Screen Holdings Co.</td>
<td>Japan</td>
<td>73</td>
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<tr>
<td>Winbond Electronics Corp.</td>
<td>Taiwan</td>
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<tr>
<td>Varian Semiconductor Equipment Associates...</td>
<td>United States</td>
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<tr>
<td>MKS Instruments Inc.</td>
<td>United States</td>
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<tr>
<td>Oerlikon Corp. AG</td>
<td>Switzerland</td>
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<tr>
<td>Brooks Automation Inc.</td>
<td>United States</td>
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</tr>
<tr>
<td>Siliconware Precision Industries Co.</td>
<td>Taiwan</td>
<td>19</td>
</tr>
</tbody>
</table>

- As a member of the JCET group of companies, STATS ChipPAC has been ranked **8th** in the Semiconductor Equipment Manufacturing scorecard, and **the highest ranking** among Outsourced Semiconductor Assembly and Test (OSAT)s in the 2016 published by the Institute of Electrical and Electronics Engineers (IEEE).
- This is **the seventh consecutive year** that the company has been recognized in the annual scorecards since 2010.
# JCET Memory Package Trends

## HVM

<table>
<thead>
<tr>
<th>PoP</th>
<th>FBGA</th>
<th>LGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>FBGA-PoPt-SD2(2D)</td>
<td>FBGA-SD4(4D+3W)</td>
<td>Micro SD 4+1 SD SiP</td>
</tr>
<tr>
<td>FBGA-PoPt-SD3(3D+2W)</td>
<td>FBGA-SD5(5D+2W)</td>
<td></td>
</tr>
<tr>
<td>FBGA-PoPt-SD4(4D+1W)</td>
<td>FBGA-SD8(8D+0W)</td>
<td>SD-SiP</td>
</tr>
<tr>
<td>FBGA-PoPt-SD4</td>
<td>VFBGA-MD6</td>
<td></td>
</tr>
<tr>
<td>WFBGA-PoPt-SD4</td>
<td>VFBGA-MD7</td>
<td></td>
</tr>
</tbody>
</table>

## Development

- **TFBGA-SD7**, 30 um WT, 1.03mm PGK T
- **TFBGA-SD8**, 35 um WT, 1.13mm PGK T
- **TFBGA-SD8**, 25 um WT, 1.13mm PGK T

XL/MC-eWLB

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L=1.4mm, T=1.2mm, V=1.0mm, W=0.8mm, U=0.65mm, X=0.50mm

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LFBGA-SD8 (NAND)

Package Features
- LFBGA 14x18mm 152LD
- NAND Die Size : 9.7x17.1mm
- Device : 20nm Non-LowK NAND
- Wafer thickness : 60um
- Mold cap: 0.84mm
- 2-lyr / 0.13mmT laminate substrate

Key Technologies
- 20nm NAND die
- 0.5mm overhang W/B with 60um die thickness
- 2-passes DA for the 8 dies stack

Current Status
- HVM since 2011
Memory Stack Die – Mixed (FBGA-SD6)
NAND + DDR + Controller

- **Package Features**
  - VFBGA-SD6 11.5x13mm 153LD
  - Nand flash Die Size: 10.33x8.12mm
  - DDR Die Size: 6.32x2.69mm
  - Controller Die Size: 6.79X1.82mm
  - 0.13mm, 3-lyr coreless substrate

- **Key Technologies**
  - 0.13T odd layer substrate handing
  - SSB loop for die to die and die to substrate
  - Warpage control w/ 3L substrate

- **Current Status**
  - HVM since 2012
FLGA-SD9 (USB)

- **Package Features**
  - FLGA 11.1x16mm
  - Memory Die Size: 8.2x11.1mm
  - Controller Die Size: 2.9x2.4mm
  - Device: 19nm Non-LowK + 65nm Lowk Controller
  - Wafer thickness: 68um x 8 dies + 150um Controller
  - 2-lyr / 0.21mmT laminate substrate

- **Key Technologies**
  - 19nm NAND die
  - 8-Die Stack with Die-to-die bonding
  - One-pass for the 8 NAND dies stack

- **Current Status**
  - HVM
Memory Stacked-Die – VFBGA-SD7

- **Package Features**
  - FBGA 11.5x13mm 221LD e-MCP
  - 4.115x1.385 (Controller) : 60um
  - 9.647x8.070 (DRAM) : 75um
  - 1.208x7.171 (Nand) : 60um
  - 9.00x8.00 (Film spacer) : 53um
  - 2-lyr / 0.41mmT laminate substrate

- **Key Technologies**
  - 60um NAND flash die
  - Film spacer application
  - Dolmen and NAND cascade structure

- **Current Status**
  - HVM from ‘2016
Fan-out Ultra Thin Memory eWLB

- 14x16mm PKG size
- 2-die Side-by-side
- Total height of ~0.31mm
- 0.3mm ball pitch
- > Over 500 IOs